



# RS780Q-LM3

VER:0.1

2009 / 6 / 8

## SCHEMATICS TABLE:

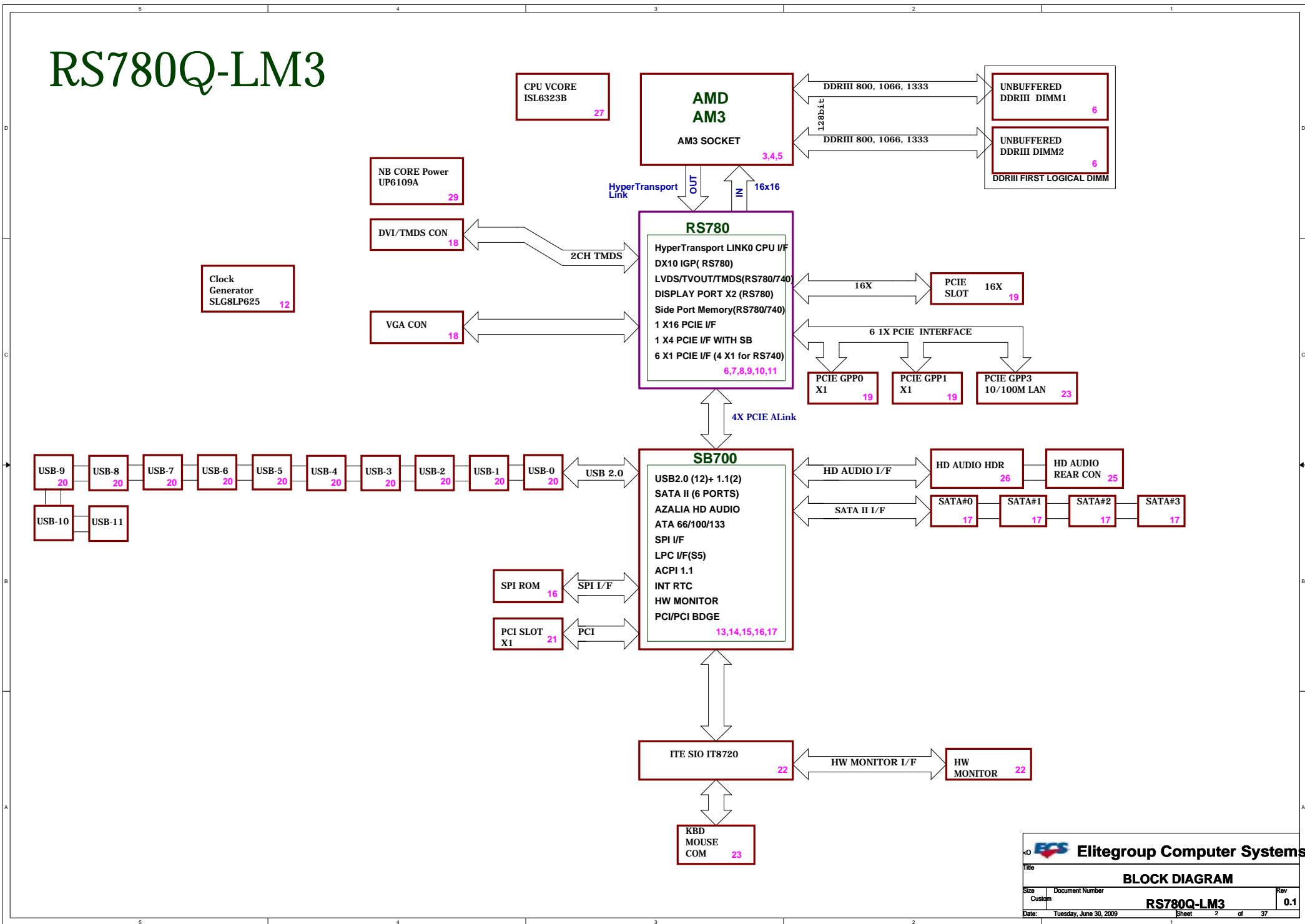
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PCB Size: 244mm\*224mm

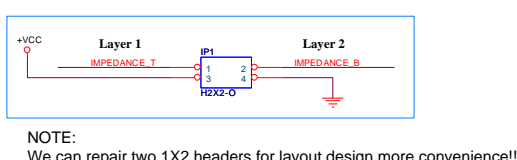
PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM  
2116, 5mils, 60 ohm

Elitegroup Computer Systems			
Title			
Cover Page			
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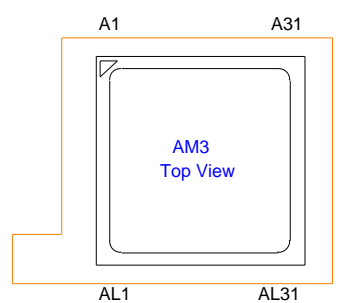
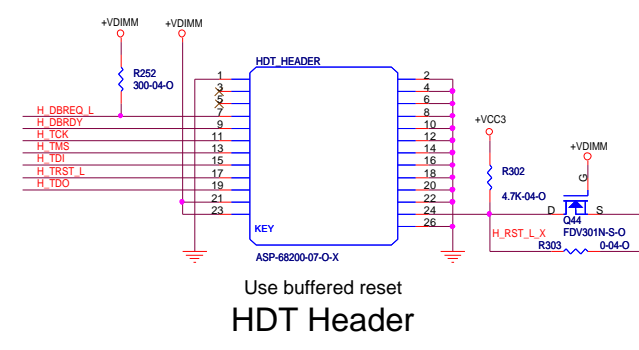
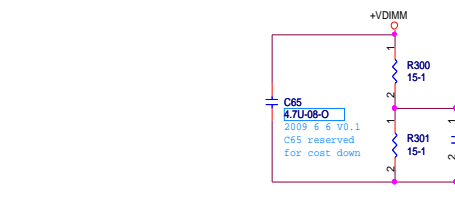
# RS780Q-LM3



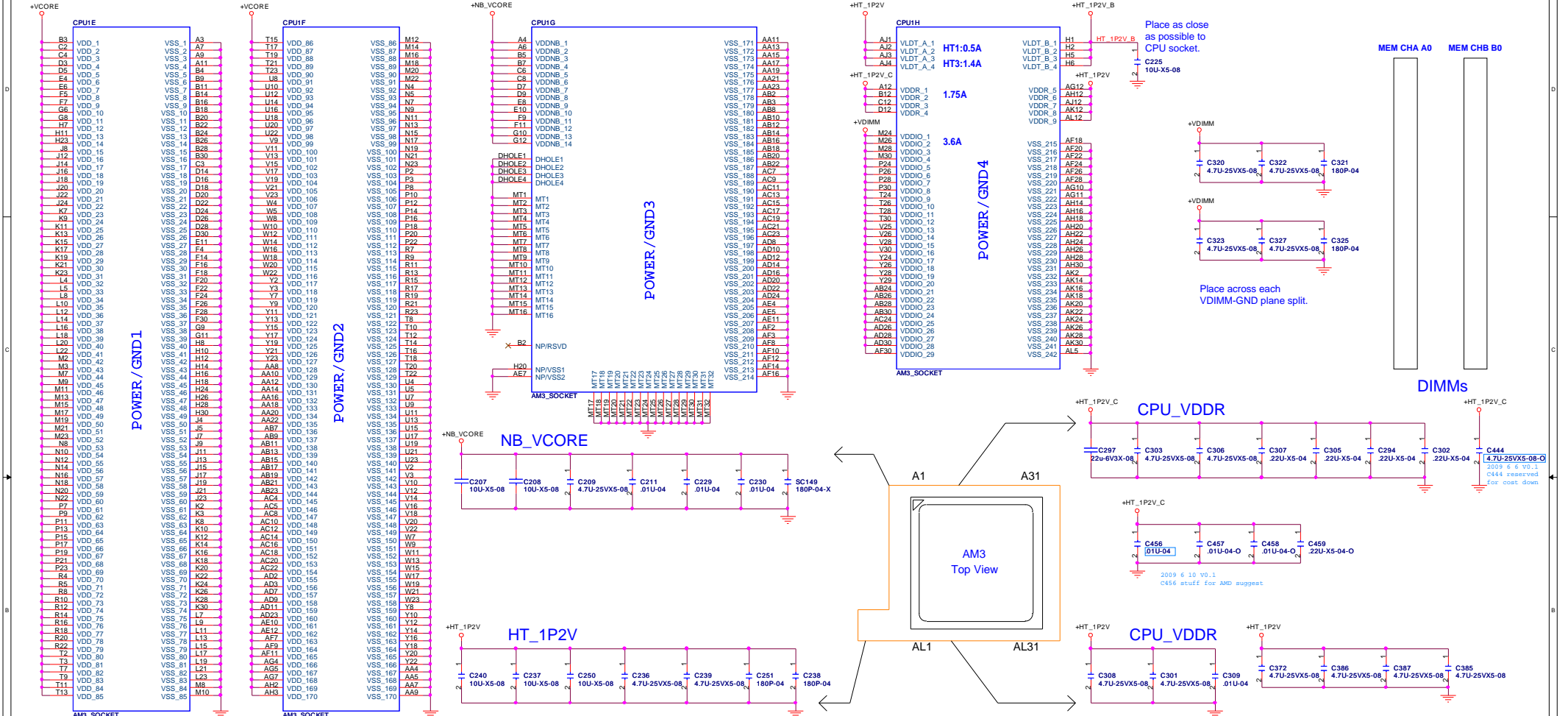
## HT LINK



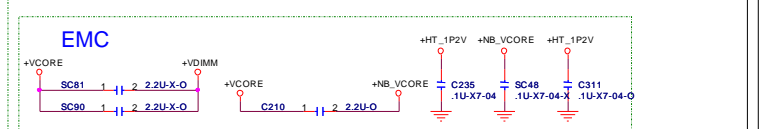
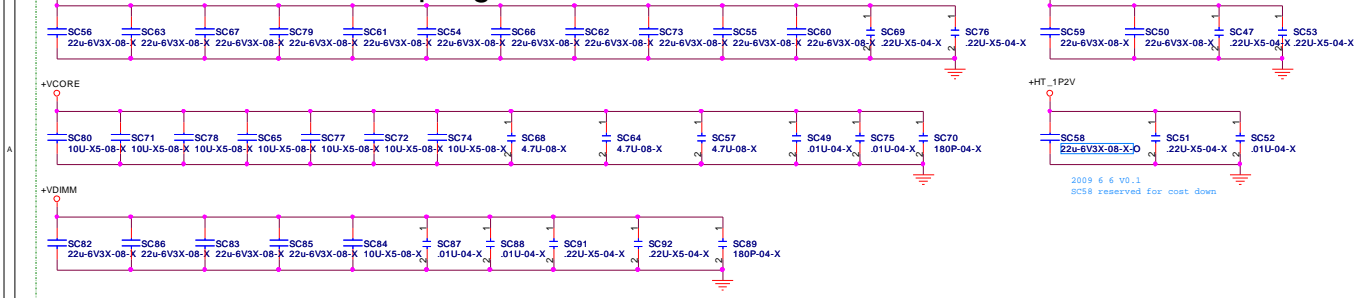
### VDDA\_2P5V for CPU PLL

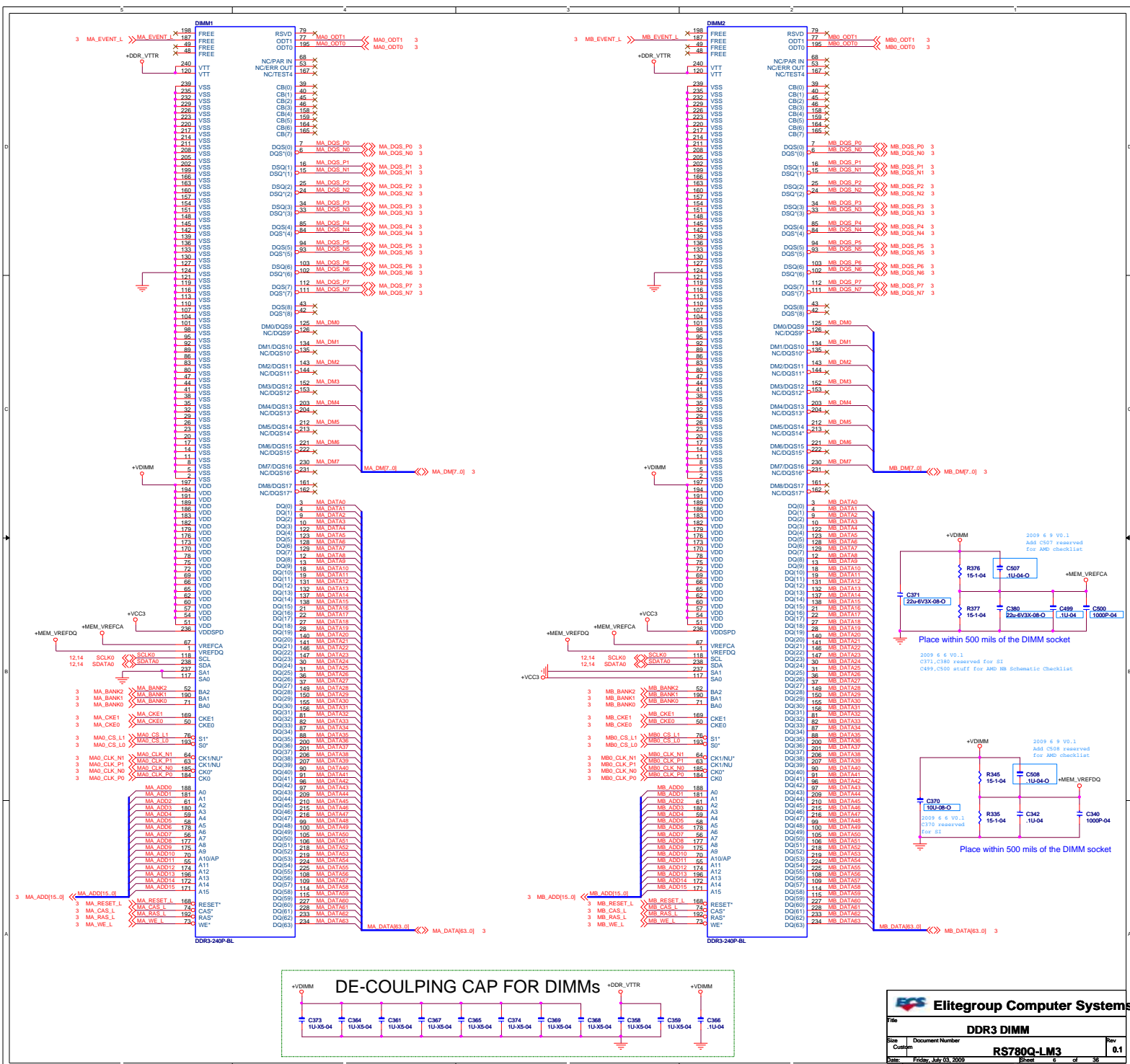


# Processor Power and Ground



## Bottom Side Decoupling





TP54 ● H\_CADOUT\_P0  
TP55 ● H\_CADOUT\_N0  
TP56 ● H\_CADOUT\_P1  
TP57 ● H\_CADOUT\_N1  
TP58 ● H\_CADOUT\_P2  
TP59 ● H\_CADOUT\_N2  
TP60 ● H\_CADOUT\_P3  
TP61 ● H\_CADOUT\_N3  
TP62 ● H\_CADOUT\_P4  
TP63 ● H\_CADOUT\_N4  
TP64 ● H\_CADOUT\_P5  
TP65 ● H\_CADOUT\_N5  
TP66 ● H\_CADOUT\_P6  
TP67 ● H\_CADOUT\_N6  
TP68 ● H\_CADOUT\_P7  
TP69 ● H\_CADOUT\_N7

STP40 ● H\_CADOUT\_P8  
STP41 ● H\_CADOUT\_N8  
STP42 ● H\_CADOUT\_P9  
STP43 ● H\_CADOUT\_N9  
STP44 ● H\_CADOUT\_P10  
STP45 ● H\_CADOUT\_N10  
STP46 ● H\_CADOUT\_P11  
STP47 ● H\_CADOUT\_N11  
STP48 ● H\_CADOUT\_P12  
STP49 ● H\_CADOUT\_N12  
STP50 ● H\_CADOUT\_P13  
STP51 ● H\_CADOUT\_N13  
STP52 ● H\_CADOUT\_P14  
STP53 ● H\_CADOUT\_N14  
STP54 ● H\_CADOUT\_P15  
STP55 ● H\_CADOUT\_N15

TP70 ● H\_CLKOUT\_P0  
TP71 ● H\_CLKOUT\_N0  
STP56 ● H\_CLKOUT\_P1  
STP57 ● H\_CLKOUT\_N1

TP72 ● H\_CTLOUT\_P0  
TP73 ● H\_CTLOUT\_N0  
STP58 ● H\_CTLOUT\_P1  
STP59 ● H\_CTLOUT\_N1

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3 H\_CADOUT\_N0  
3 H\_CADOUT\_P1  
3 H\_CADOUT\_N1  
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3 H\_CADOUT\_N2  
3 H\_CADOUT\_P3  
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3 H\_CADOUT\_N15

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3 H\_CLKOUT\_N1

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3 H\_CTLOUT\_N0  
3 H\_CTLOUT\_P1  
3 H\_CTLOUT\_N1

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H\_CLKOUT\_N1

H\_CTLOUT\_P0  
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H\_CTLOUT\_N1

Y25  
Y24  
Y22  
Y23  
Y25  
Y24  
U24  
U25  
T25  
T24  
P22  
P23  
P24  
N24  
N25

AC24  
AC25  
AB25  
AB24  
AA24  
AA25  
Y22  
Y23  
W21  
W20  
V21  
V20  
U20  
U21  
U19  
U18

T22  
T23  
AB23  
AA22

M22  
M23  
R21  
R20

NB1A

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HT\_RXCAD0N  
HT\_RXCAD1P  
HT\_RXCAD1N  
HT\_RXCAD2P  
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HT\_RXCLK1N

HT\_RXCTL0P  
HT\_RXCTL0N  
HT\_RXCTL1P  
HT\_RXCTL1N

HT\_RXCALP  
HT\_RXCALN

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT\_TXCAD0P  
HT\_TXCAD0N  
HT\_TXCAD1P  
HT\_TXCAD1N  
HT\_TXCAD2P  
HT\_TXCAD2N  
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HT\_TXCTL0P  
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HT\_TXCALP  
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D24  
D25  
E24  
E25  
F24  
F25  
F23  
F22  
H23  
H22  
J25  
J24  
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K22

F21  
G21  
G20  
H21  
J20  
J21  
J18  
K17  
L19  
J19  
M19  
L18  
M21  
P21  
P18  
M18

H24  
H25  
L21  
L20

M24  
M25  
P19  
R18

B24  
B25

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HT\_TXCALP  
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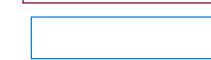
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HT\_TXCALP  
HT\_TXCALN

080907 add ICT test point

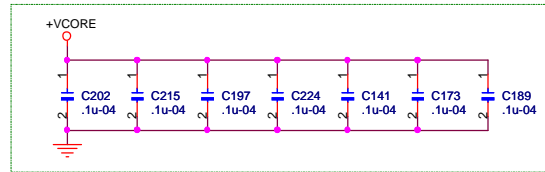
R148 1 2 301-1-04



2009 6 6 V0.1  
Del R153,R142  
for not Co-Lay RS740

2009 6 6 V0.1  
Del SR32,SR33  
for not Co-Lay RS740

### HT LINK STITCHING CAPS.

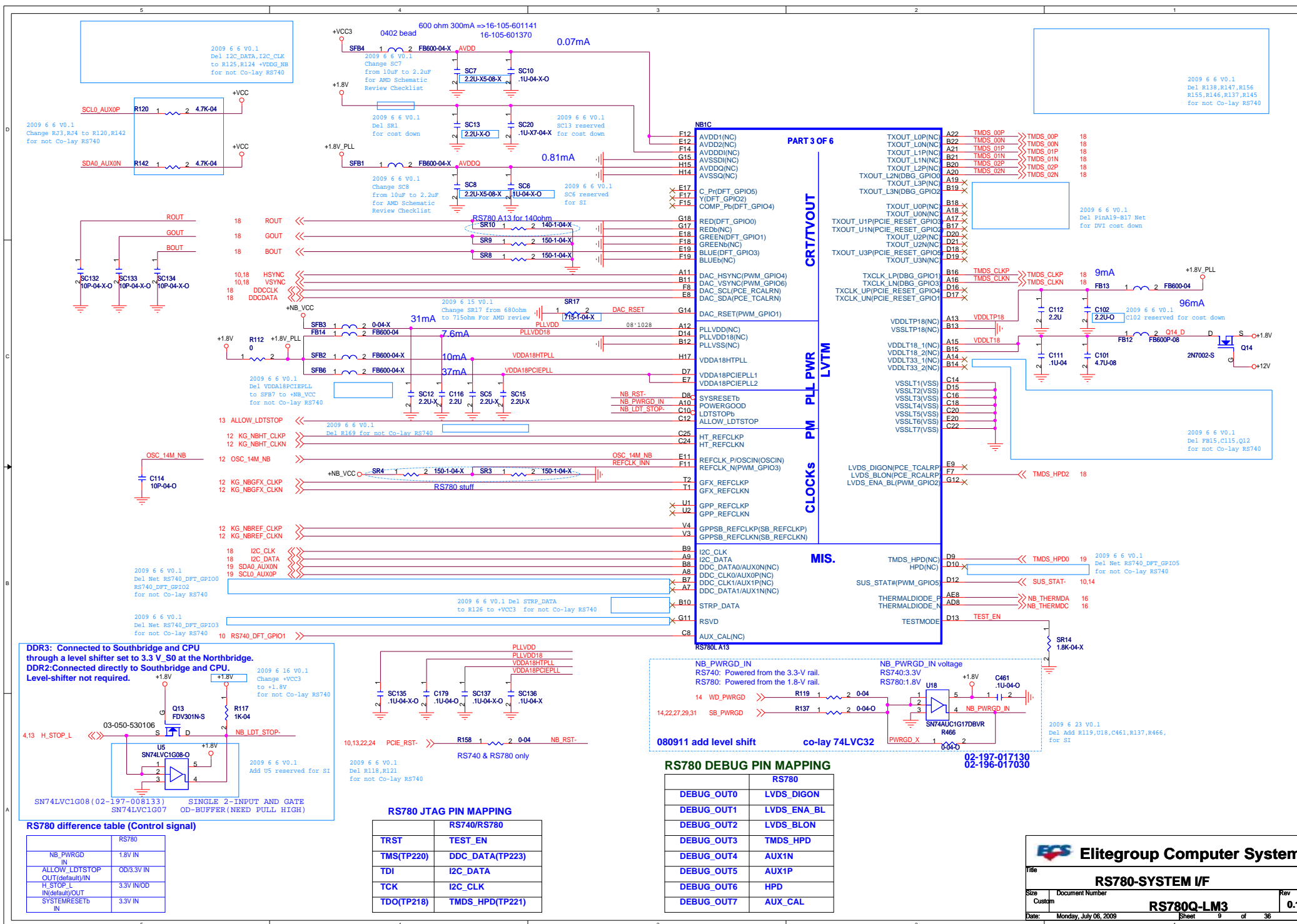


<b>ECS</b> Elitegroup Computer Systems		
Title <b>RS780-HT LINK I/F</b>		
Size Custom	Document Number <b>RS780Q-LM3</b>	Rev <b>0.1</b>
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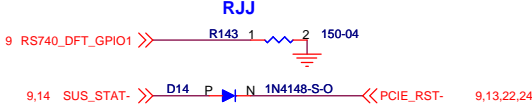






# RS740/RS780 STRAPS

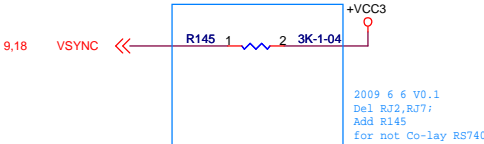
Note: for RS780, change RJJ to 150R as AUX\_CAL, place close to pin C8



Note: RS740\_DFT\_GPIO1: Made provision for external pull-down which is not installed by default. Northbridge has an internal pull-up for bypassing EEPROM strapping and using default values for RS740

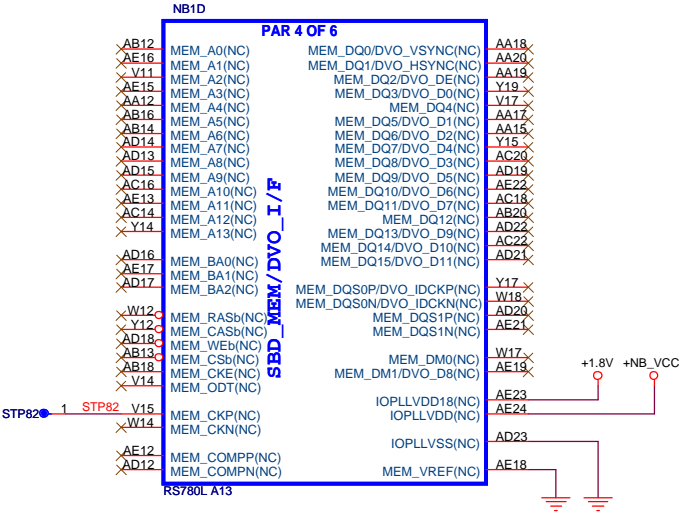
## RS740/RS780: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740: pin DFT\_GPIO1  
RS780: pin SUS\_STAT#

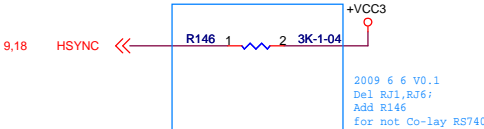


## RS740/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO  
1 : Disable (RS740/RS780); Enable (RX780)  
0 : Enable (RS740/RS780); Disable (RX780)  
RS740: pin DFT\_GPIO5  
RS780: pin VSYNC



2009 6 6 V0.1  
Del SR2,SR5,R143  
for not Co-lay RS740



## RS740/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory  
1. Disable (RS740/RS780)  
0 : Enable (RS740/RS780)  
RS740: pin DFT\_GPIO0  
RS780: pin HSYNC

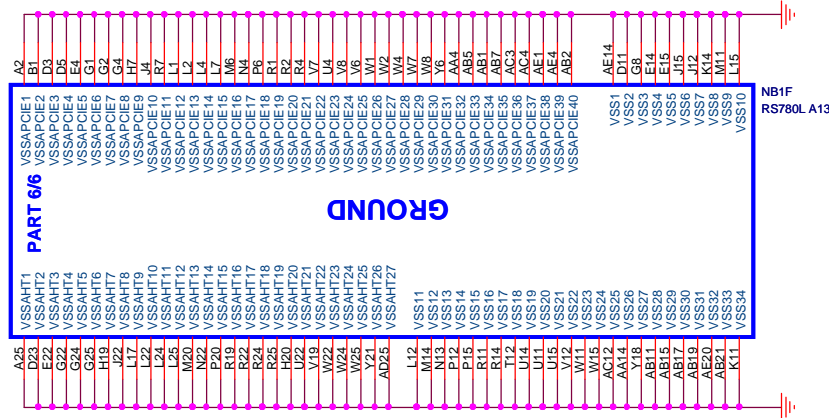
## RS780: STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

Enables Test debug bus using PCIE bus  
1. Disable (can be enabled thru nbcfg register)  
0 : Enable  
RS780: configurable thru register setting only  
RS740: Not supported

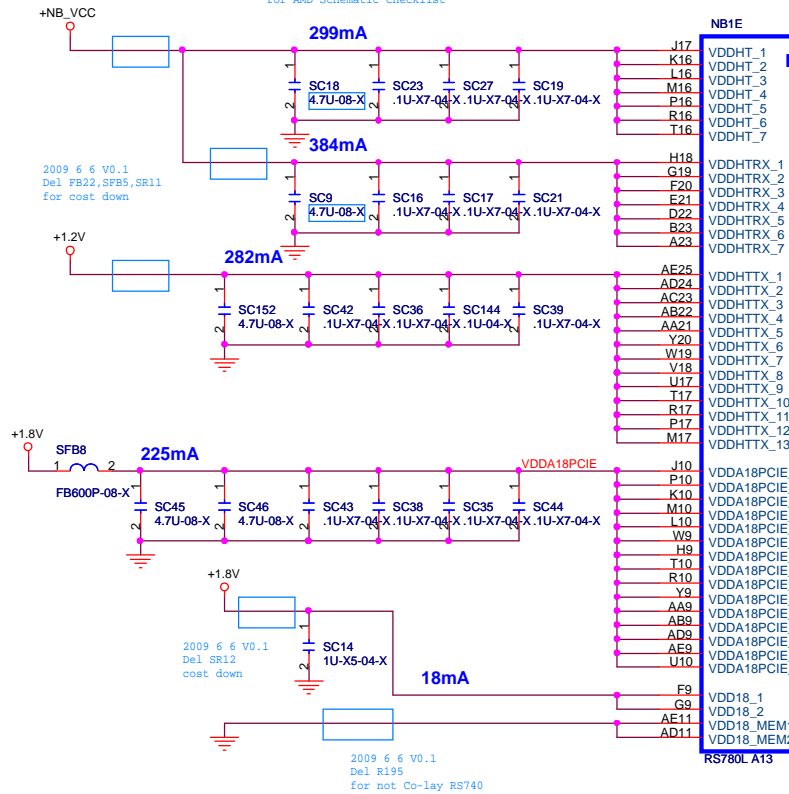


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Title			RS780-SPMEM/STRAPS
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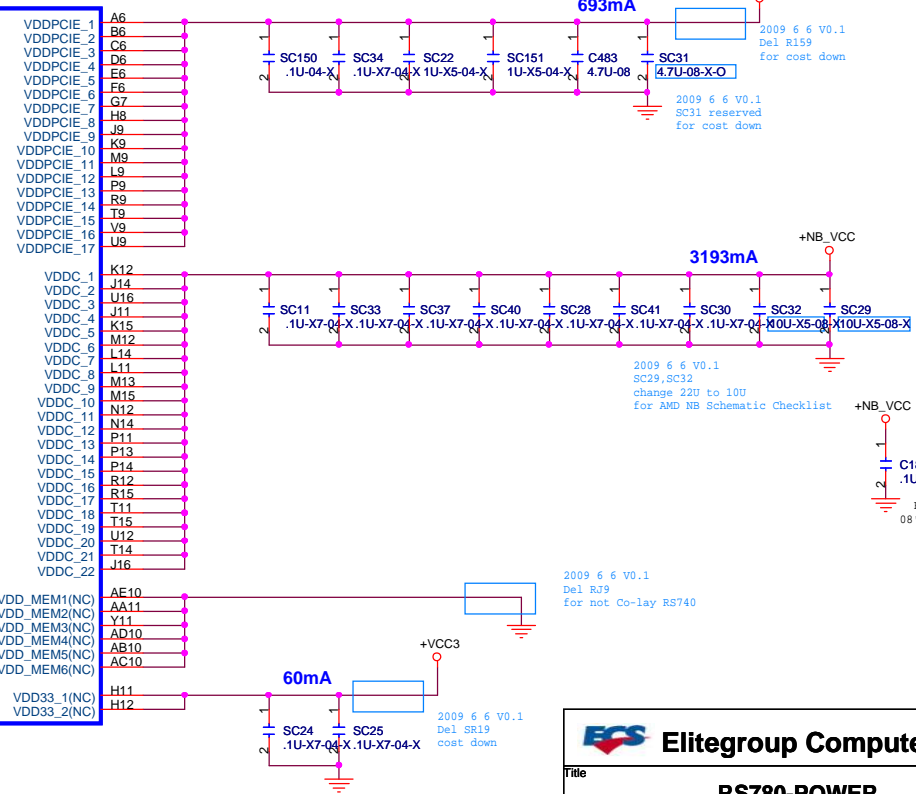
2009 6 10 V0.1  
change SC18+SC9 from 220 to 4.7u  
for AMD Schematic Checklist



2009 6 6 V0.1  
Del R195  
for not Co-Lay RS740

RS740/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RS780	PIN NAME	RS740	RS780
VDDHT	NC	+1.1V	IOPLLVD	+1.2V	+1.1V
VDDHTRX	NC	+1.1V	AVDD	+3.3V	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	+1.8V	+1.8V
VDDA18PCIE	NC	+1.8V	AVDDQ	+1.8V	+1.8V
VDD18	+1.8V	+1.8V	PLLVD	+1.2V	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	+1.8V	+1.8V
VDDPCIE	+1.2V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V
VDDC	+1.2V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	+1.8V	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	+1.8V
VDD33	+3.3V	+3.3V	VDDLTP18	+1.8V	+1.8V
IOPLLVD18	+1.8V	+1.8V	VDDLTP18	+1.8V	+1.8V

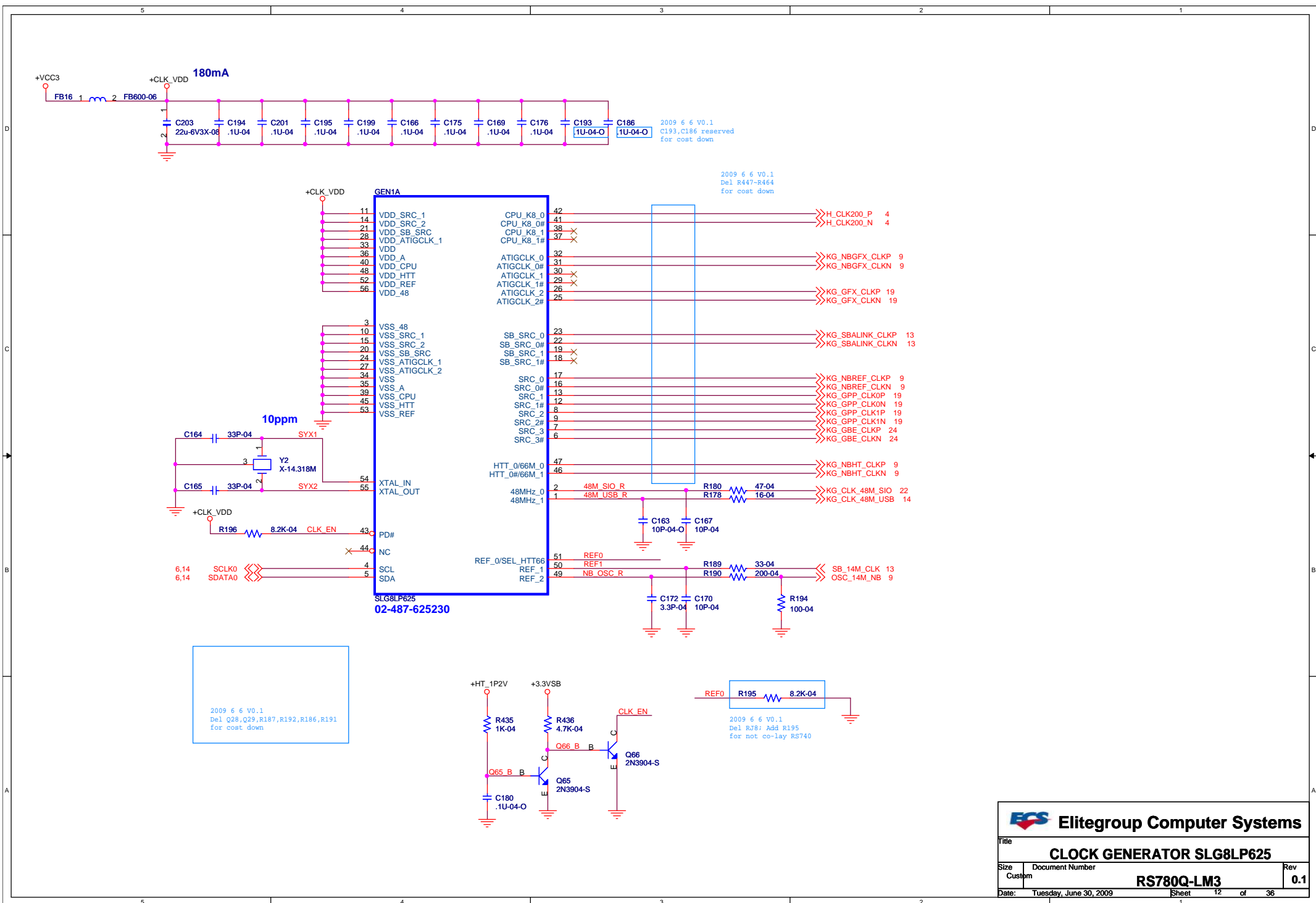


**Elitegroup Computer Systems**

Title: **RS780-POWER**

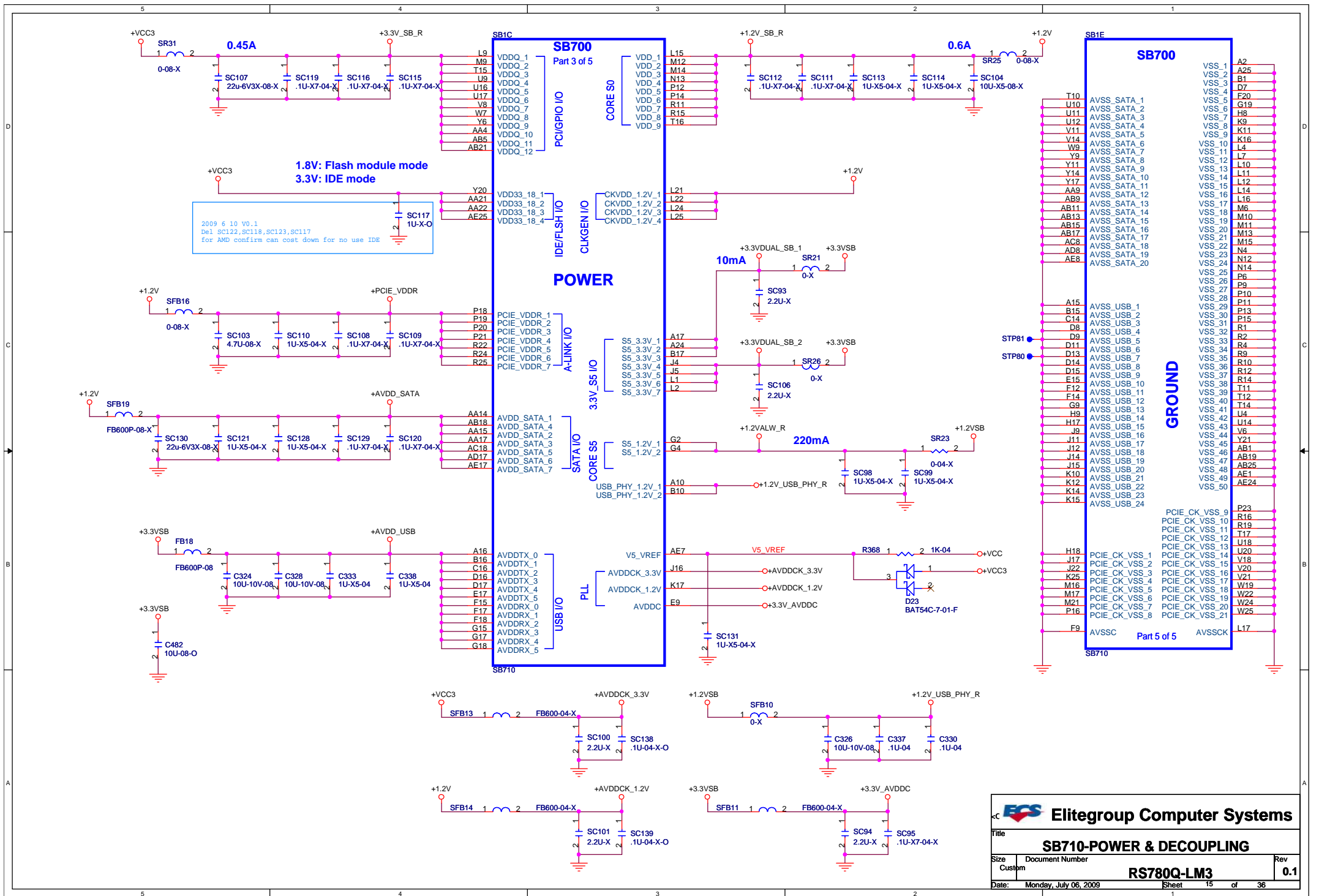
Size: Custom Document Number: **RS780Q-LM3** Rev: **0.1**

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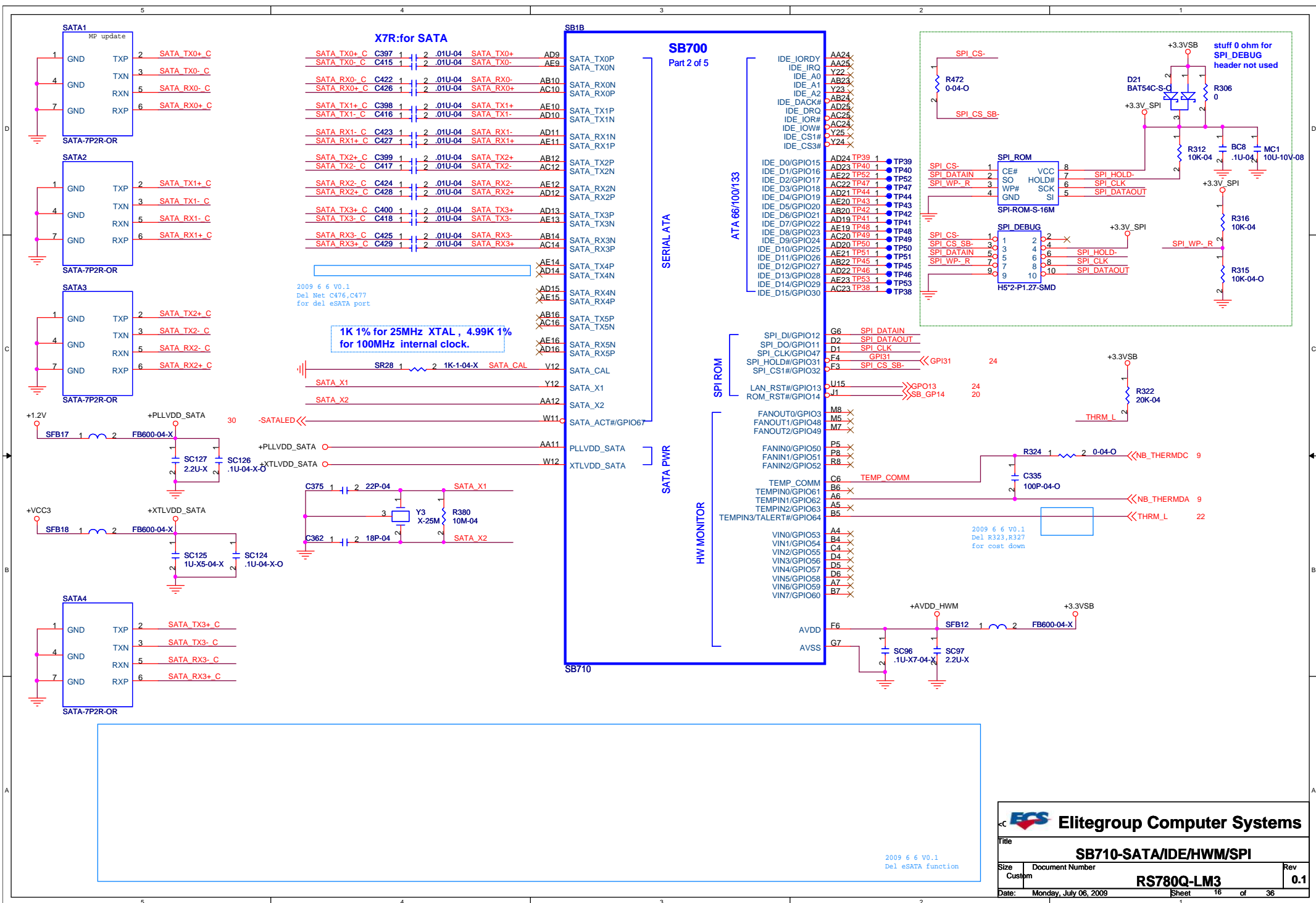


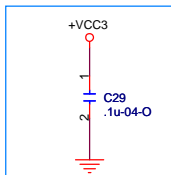




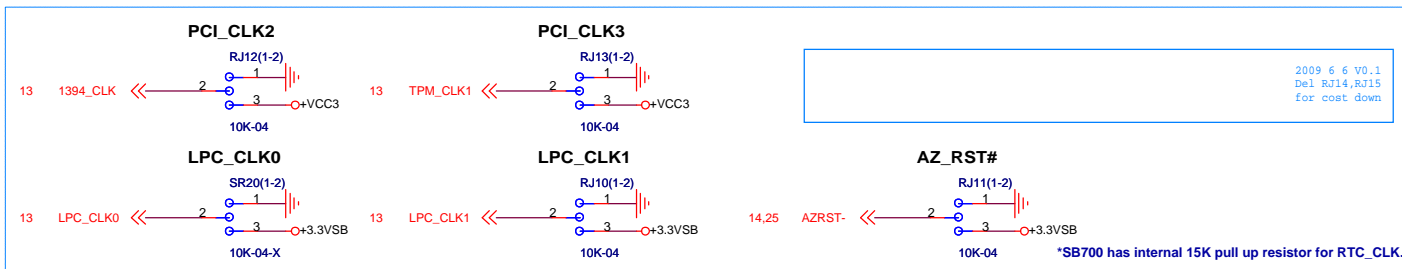








2009 6 29 V0.1  
Add C29 reserved  
for EMI



2009 6 6 V0.1  
Del RJ14,RJ15  
for cost down

## REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3			LPC_CLK0	LPC_CLK1	AZ_RST#
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS			ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT

STRAP of ROM select—Default is SPI ROM

IMC\_GPIO17



IMC\_GPIO16



IMC\_GPIO17 IMC\_GPIO16

ROM TYPE:

H, H = Reserved

H, L = SPI ROM DEFAULT

L, H = LPC ROM

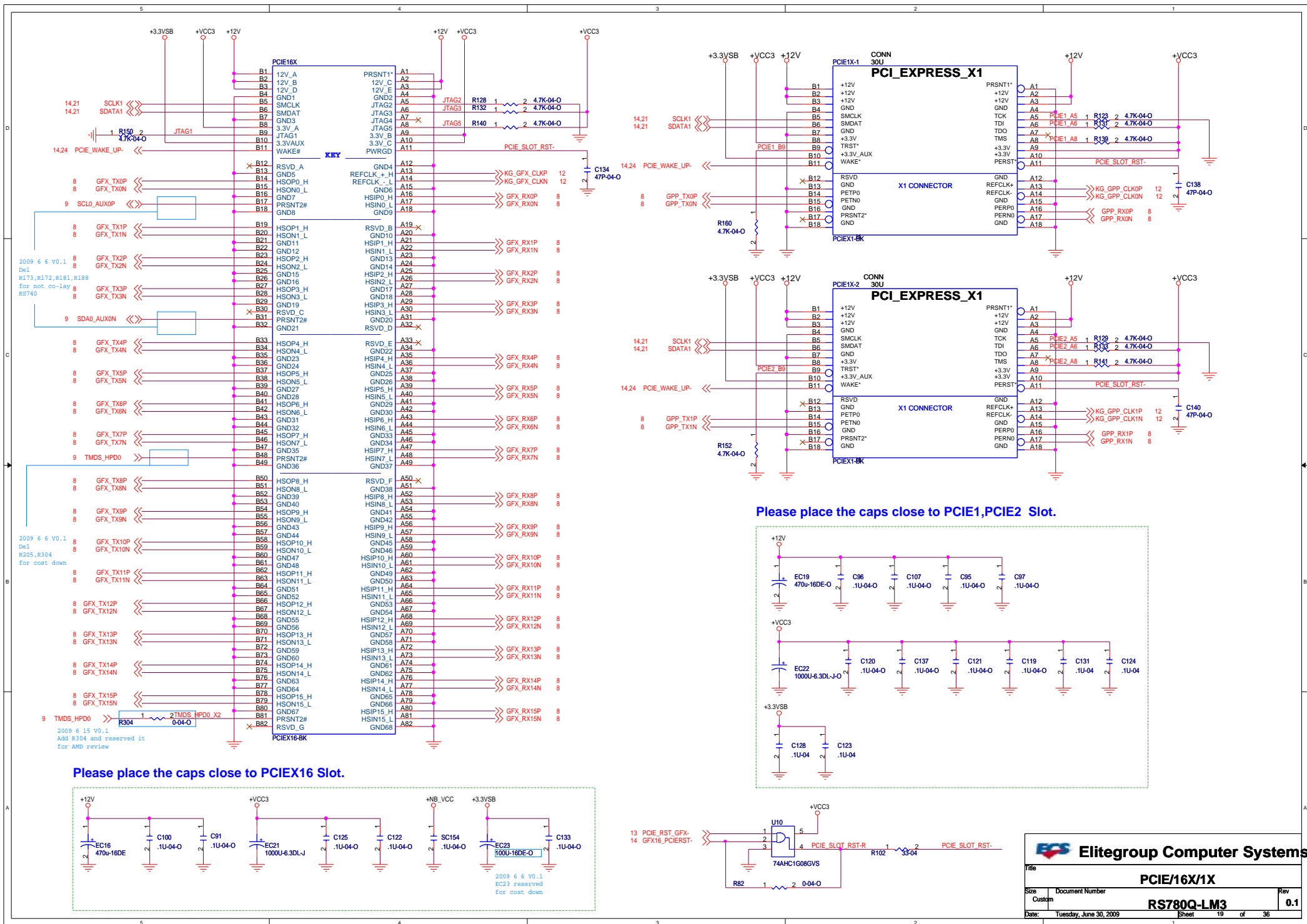
L, L = FWB ROM



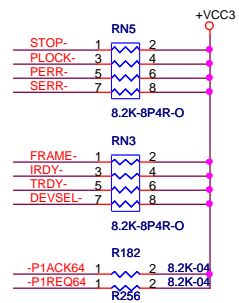
Elitegroup Computer Systems

Title			SB710-STRAPS		
Size	Document Number	Rev			
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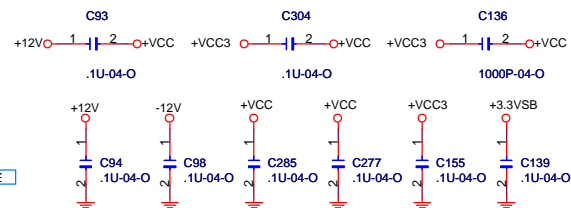


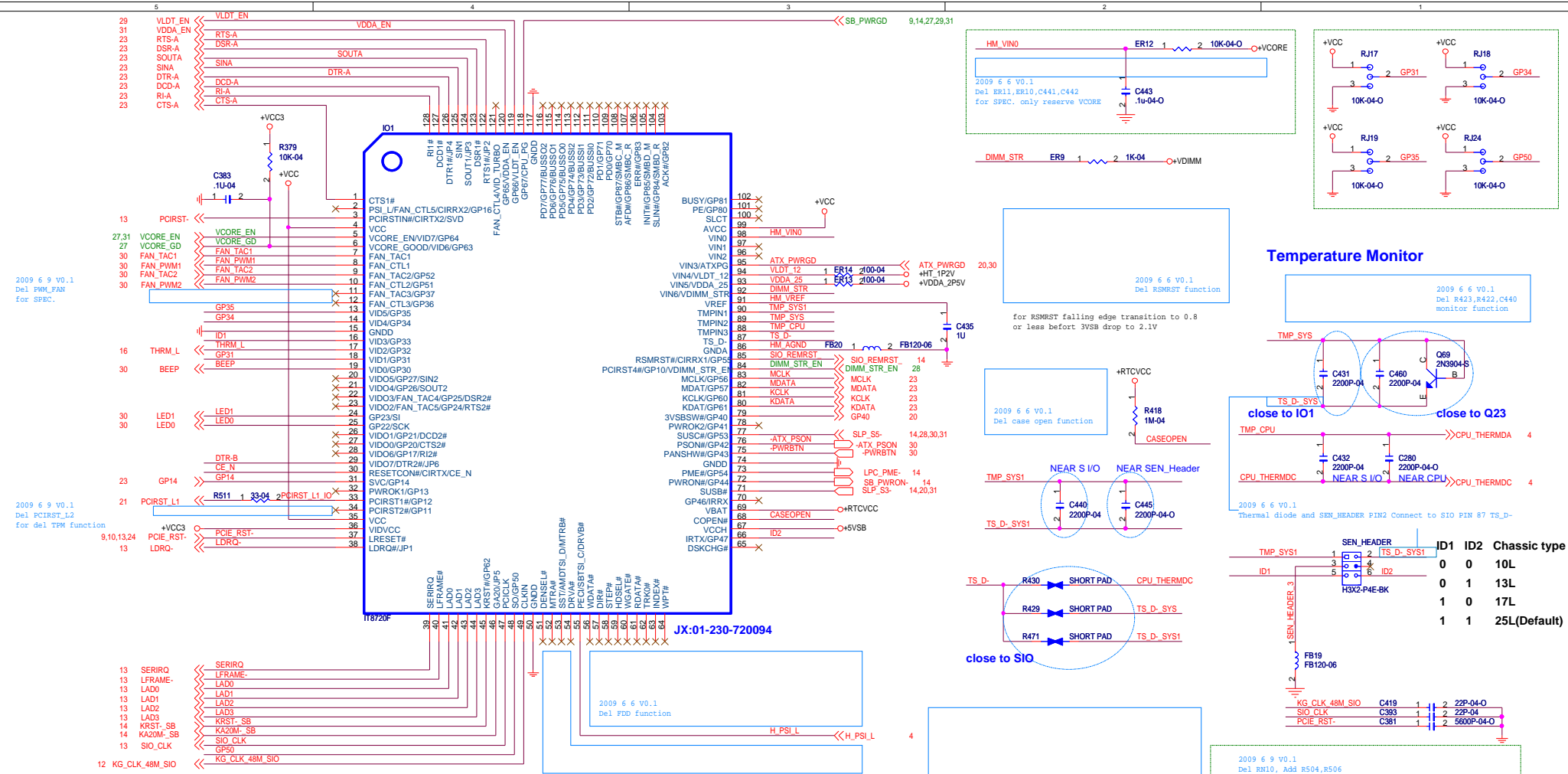
PCIRST\_L1 BC4 1 2 47P-04-O

PCI CLK1 C143 1 2 47P-04-O

EC42  
22U-25DE

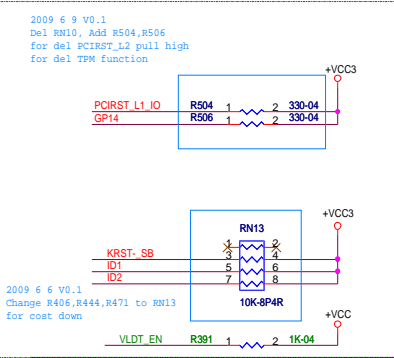
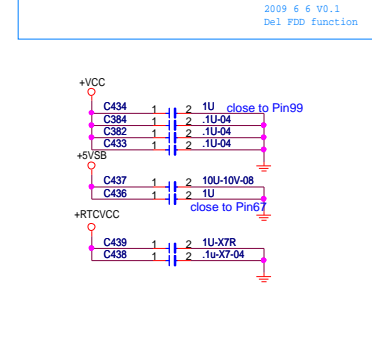
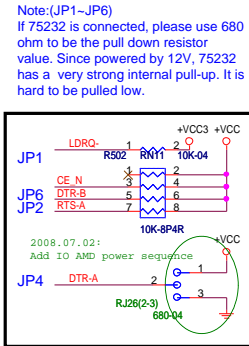
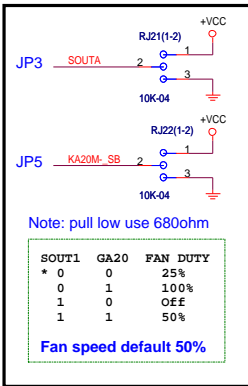
2009 6 6 V0.1  
Change EC42  
1000U to 22U  
for cost down





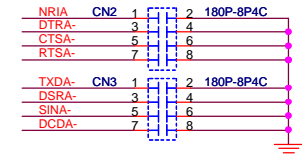
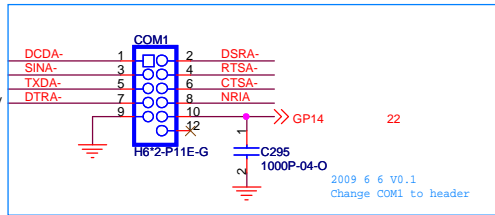
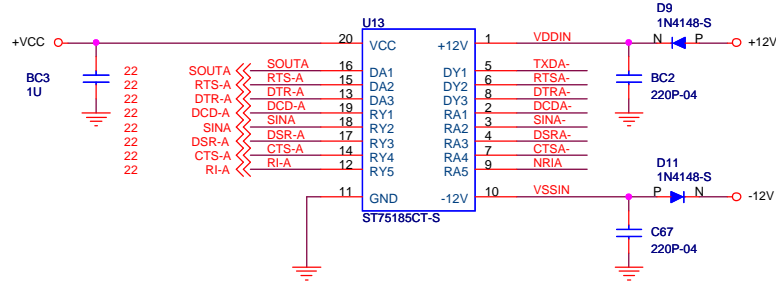
IT8720 Power On Strapping Options

Symbol	value	Description
JP3	Flashseg1_EN	1 Disabled.
Pin 124	Flash I/F Address Segment 1 is enabled	0 Flash I/F Address Segment 1 is enabled
JP4	K8PWR_EN	1 K8 power sequence function is disabled
Pin 126	K8 power sequence function is enabled	0 K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11 The default value of EC Index 15h/16h/17h is 40h
Pin 124	The default value of EC Index 15h/16h/17h is 7Fh(Fan off )	10 The default value of EC Index 15h/16h/17h is 00h(Fan full speed )
& 46	The default value of EC Index 15h/16h/17h is 20h	00 The default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin46	Enable WDT to rest PWROK	0 Enable WDT to rest PWROK
JP2/JP6	SVID_EN	11 Disable VID/SVID out pins
Pin122/Pin29	For Intel Platform Enable VIDO0-VID07 output pins.	01 For Intel Platform Enable VIDO0-VID07 output pins.
	For AMD Platform(always serial output) Enable SVD(Pin3)/SVC(Pin31)Output pins	10 For AMD Platform(always serial output) Enable SVD(Pin3)/SVC(Pin31)Output pins
	For AMD Platform(Serial-IN/Serial-Out and Parallel-IN/Parallel-Out It is selected by CPU	00 For AMD Platform(Serial-IN/Serial-Out and Parallel-IN/Parallel-Out It is selected by CPU

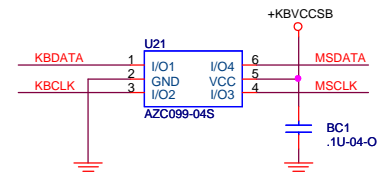
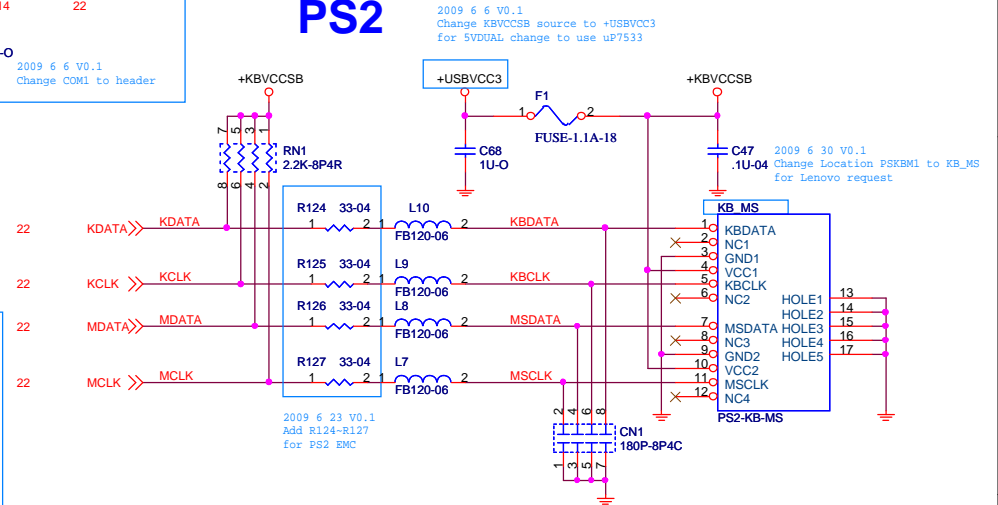




# COM



# PS2

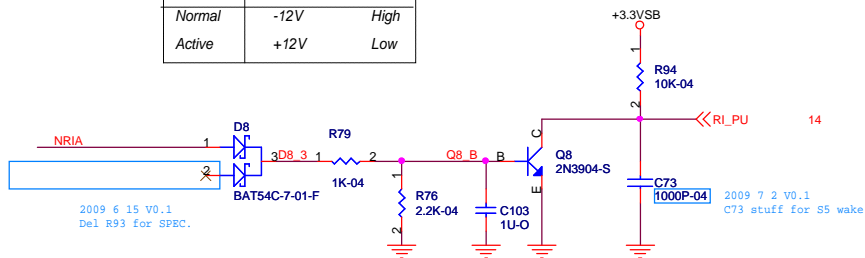


Close to PSKBM1 connector

2009 6 15 V0.1  
Del U18,C300,C299,BC5,COM2 for SPEC.

2009 6 15 V0.1  
Del CN4,CN5 for SPEC.

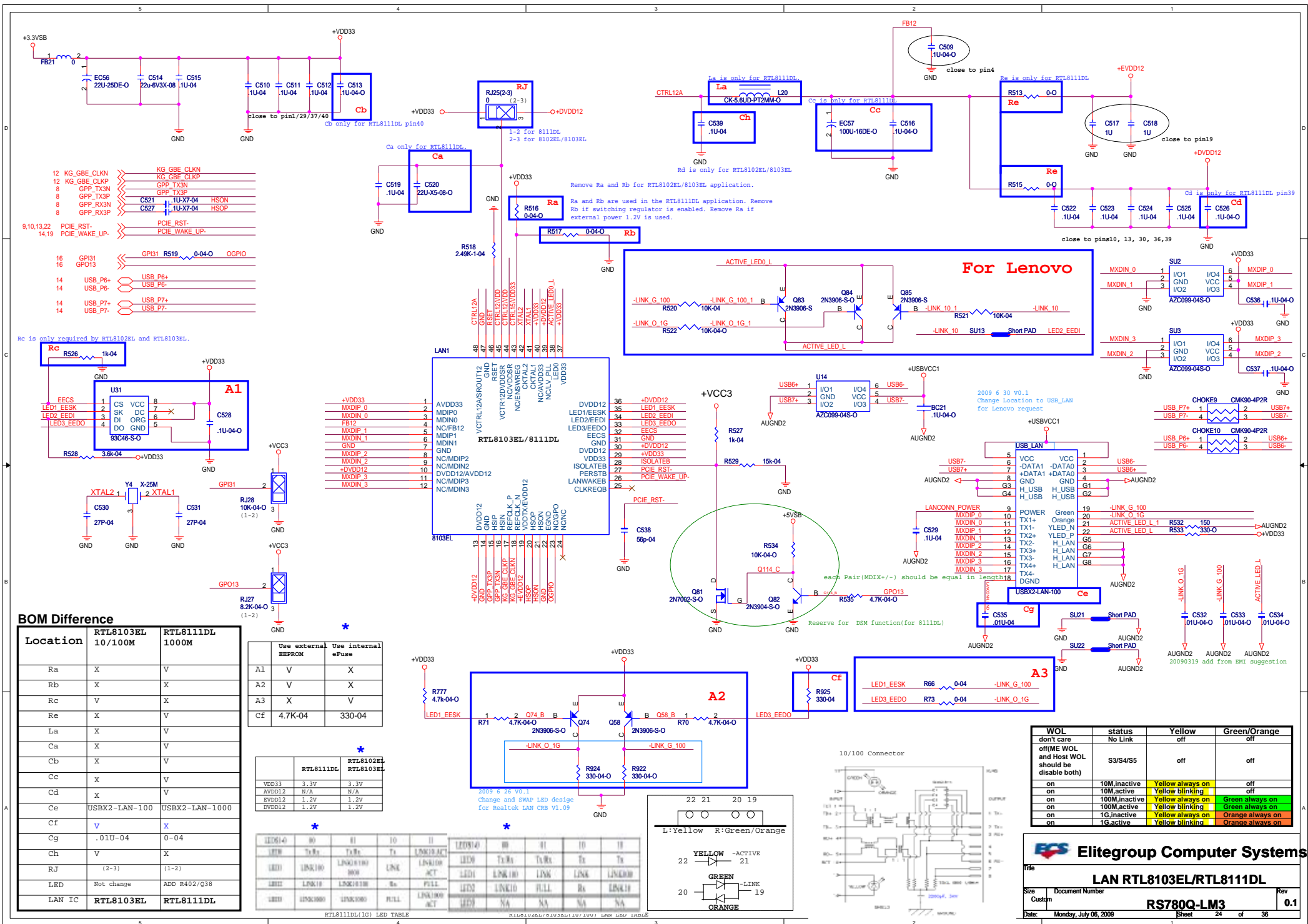
	NR1A	R#
Normal	-12V	High
Active	+12V	Low



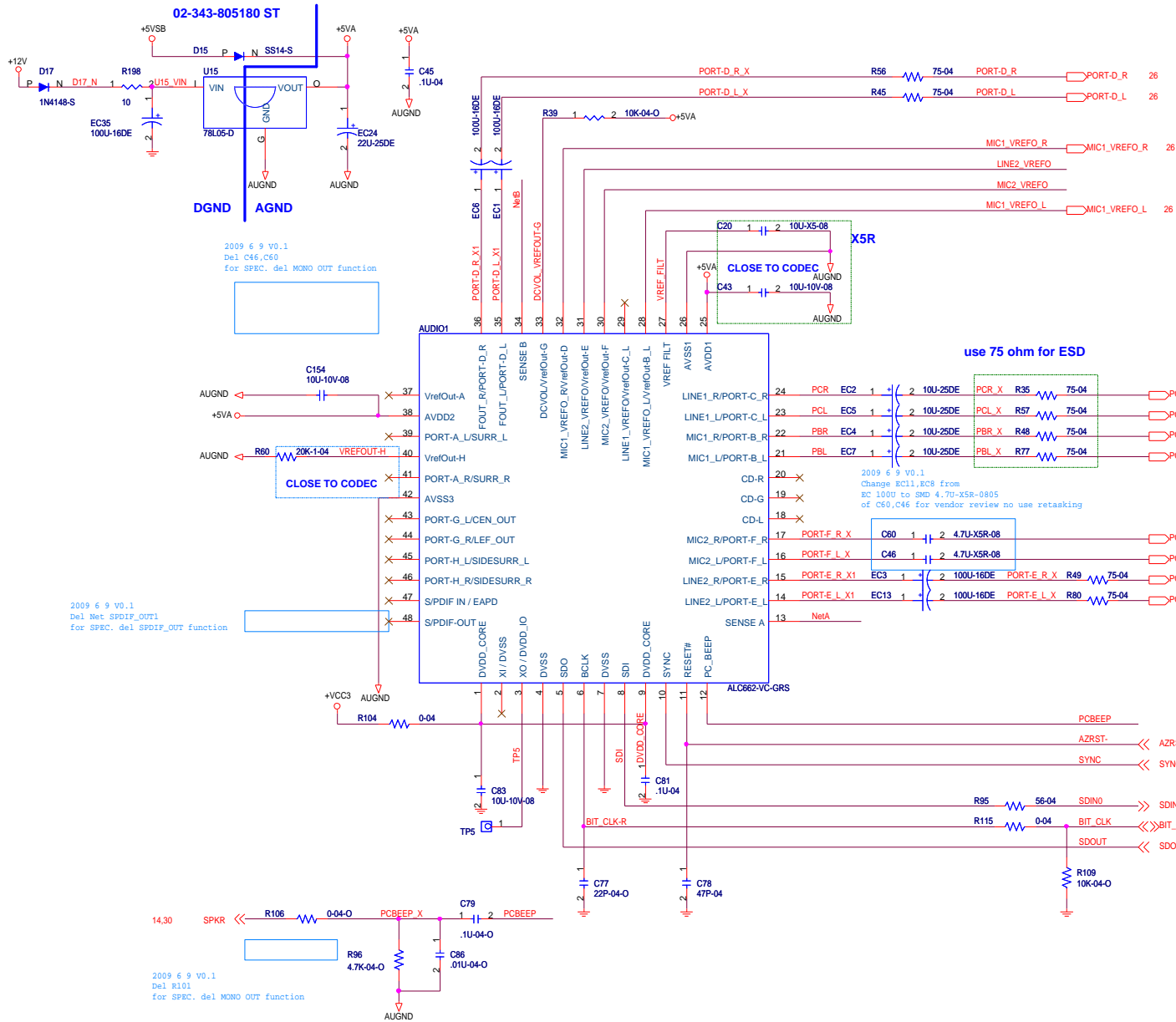
2009 6 15 V0.1  
Del R93 for SPEC.

2009 7 2 V0.1  
C73 stuff for S5 wake

Title		
PS2 / COM PORT		
Size	Document Number	Rev
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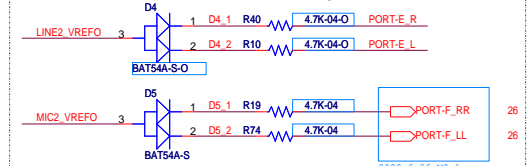


WOL	status	Yellow	Green/Orange
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	\$3/\$4/\$5	off	off
on	10M_inactive	Yellow always on	off
on	10M_active	Yellow blinking	off
on	100M_inactive	Yellow always on	Green always on
on	100M_active	Yellow blinking	Green always on
on	1G_inactive	Yellow always on	Orange always on
on	1G_active	Yellow blinking	Orange always on



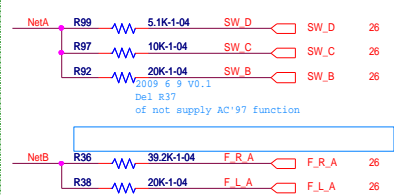
2009 6 9 V0.1  
Change R40,R10,R19,R74 from  
2.2K to 4.7K and reserved D4,R40,R10  
for vendor review no use retasking

### Verfout bias for stereo microphone.



Placement near to codec

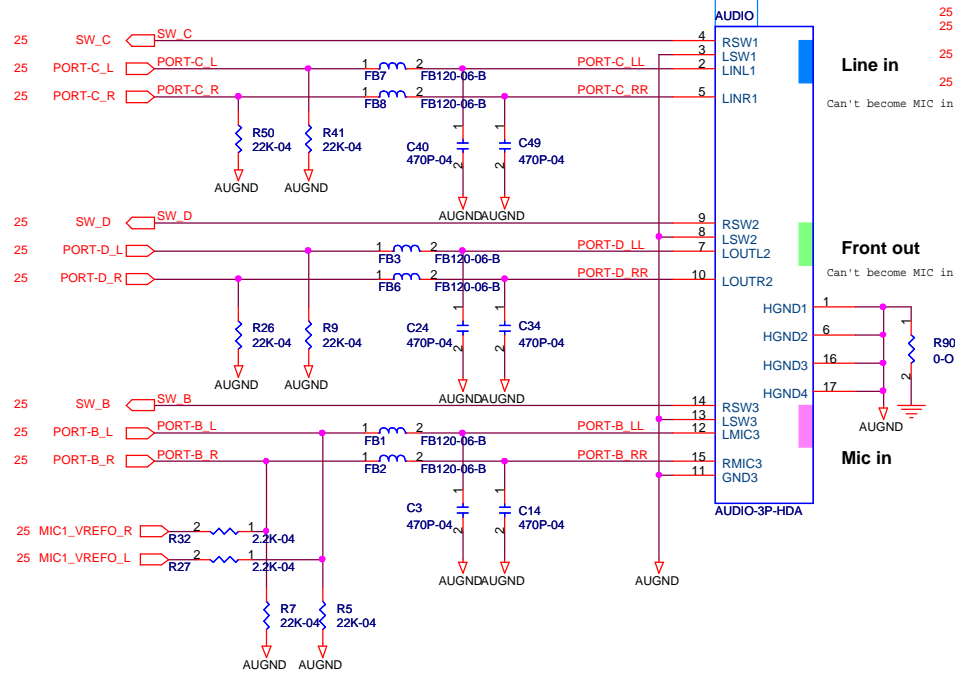
### Resistors Networks



Placement near to codec

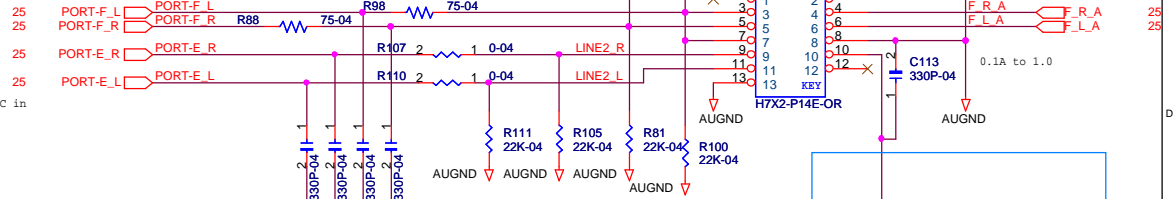
080825 remove CD-IN function.

2009 6 30 V0.1  
Change Location to AUDIO  
for Lenovo request



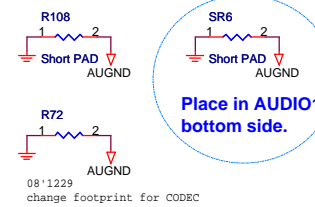
2009 6 9 V0.1  
Del R3, R2, C2, C1, R1, R6, C19, U1,  
R4, D3, MONO\_OUT, D2, C22  
for SPEC. del MONO OUT function

2009 6 26 V0.1  
Change net connect  
for vendor review

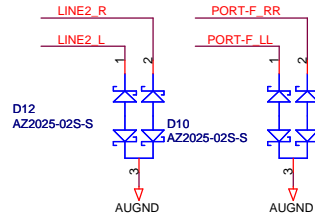
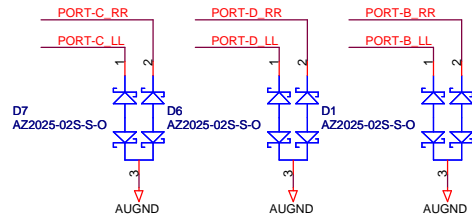


NEAR F\_AUDIO

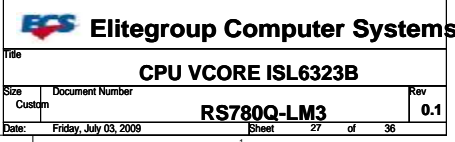
080911 Realtek recommend



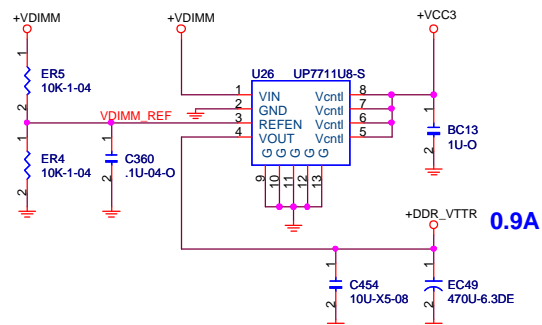
Place in AUDIO1  
bottom side.



2009 6 9 V0.1  
Del Q1, R114, C104, R113  
of not supply AC'97 function



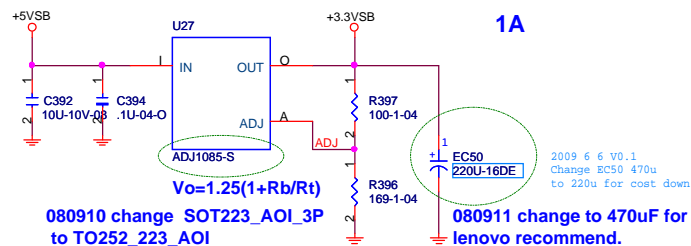
## DDR\_VTTR



0.9A

## 3VSB

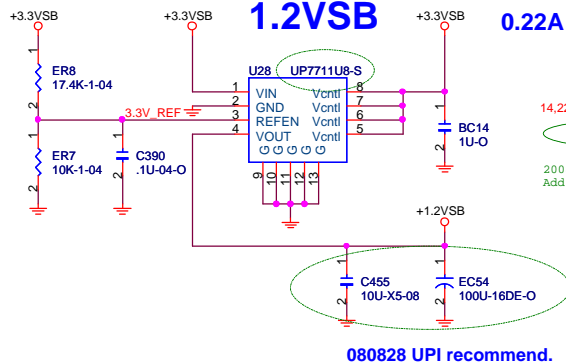
080828 UPI recommend.



1A

## 1.2VSB

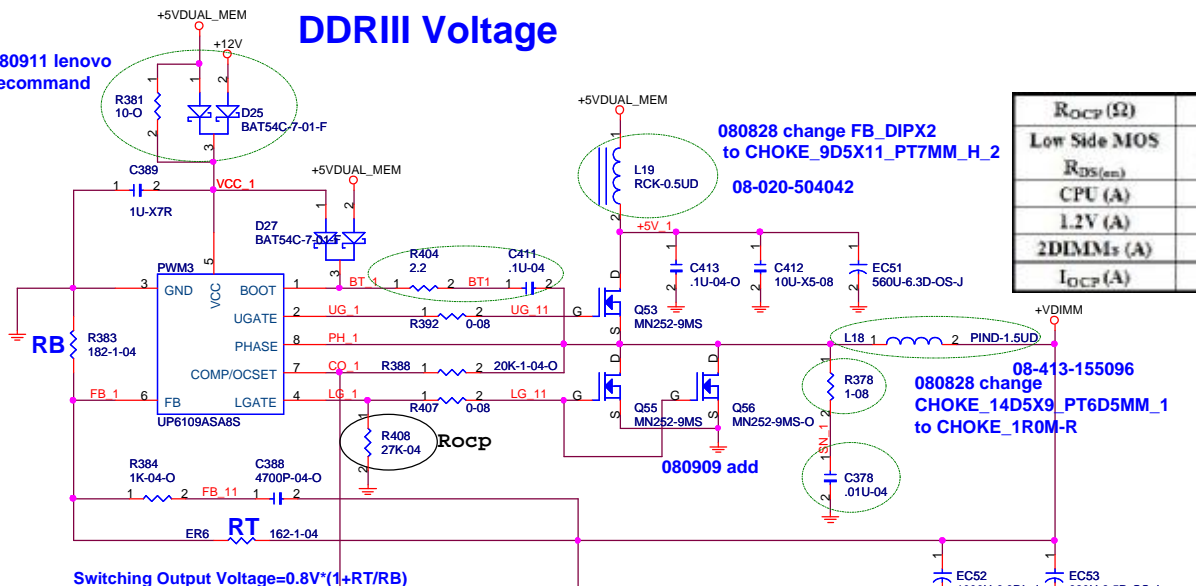
0.22A



080828 UPI recommend.

## DDR3 Voltage

080911 lenovo  
recommand



$R_{OCP}(\Omega)$	27K
Low Side MOS	9mΩ
$R_{DS(on)}$	
CPU (A)	3.6
1.2V (A)	5.3
2DIMMs (A)	6
$I_{OCP}(A)$	25

080828 change FB\_DIPX2  
to CHOKE\_9D5X11\_PT7MM\_H\_2  
08-020-504042

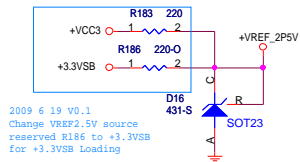
08-413-155096  
080828 change  
CHOKE\_14D5X9\_PT6D5MM\_1  
to CHOKE\_1R0M-R

Switching Output Voltage=0.8V\*(1+RT/RB)

14,22,30,31 SLP\_S5-  
22 DIMM\_STR\_EN  
2008.07.02:  
Add IO AMD power sequence

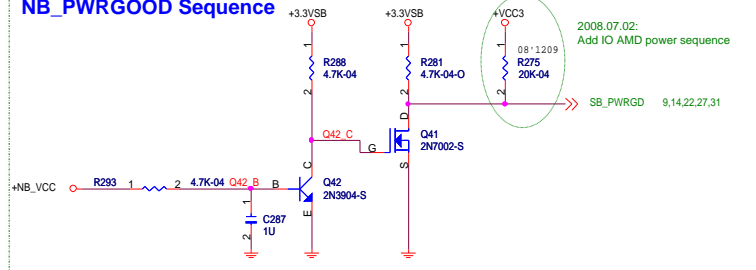
+VDIMM:  
Low disable  
High enable

**VREF 2.5V**



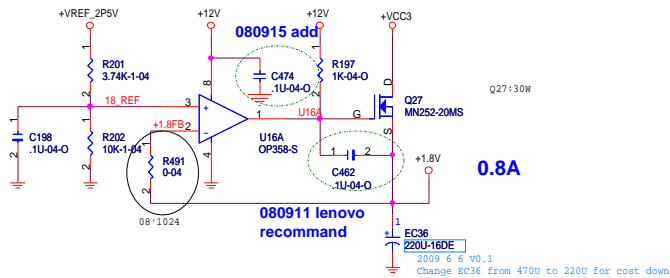
```
2009 6 19 V0.1
Change VREF2.5V source
reserved R186 to +3.3VSB
for +3.3VSB Loading
```

### NB\_PWRGOOD Sequence



2008.07.02:  
Add IO AMD power sequence

>> SB\_PWRGD 9,14,22,27,31

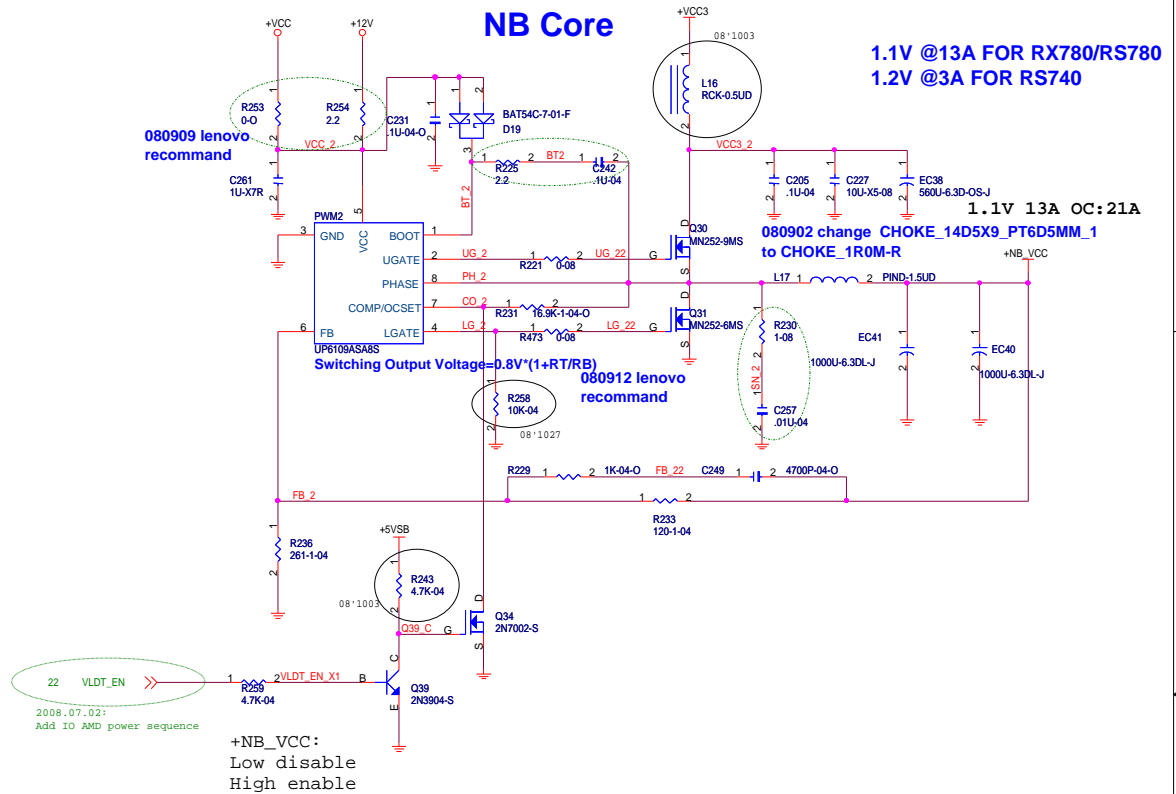


+1.2V:  
Low disable  
High enable

2008.07.02: 4.  
Add IO AMD power sequence

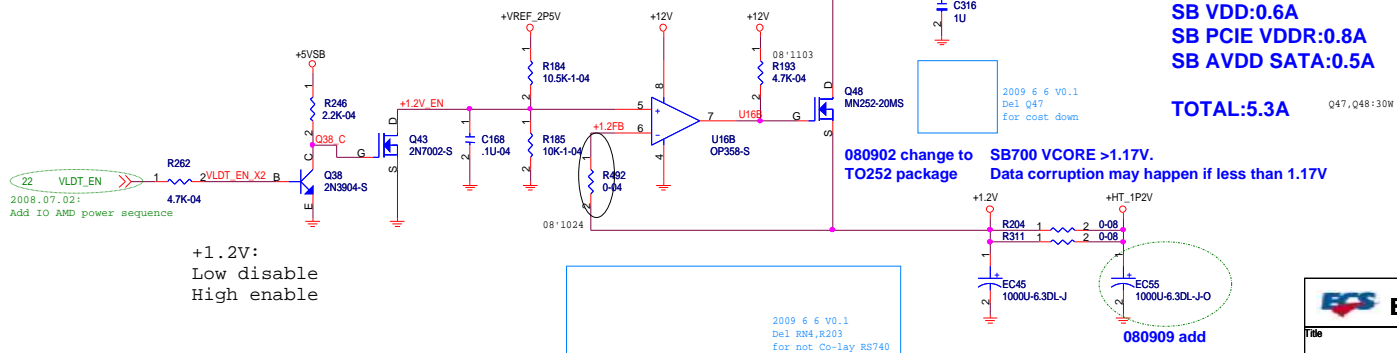
2009 6 6 V0.1  
Change EC36 from 470U to 220U for cost down

## NB Core



```
+NB_VCC:
Low  disable
High enable
```

## RS780 USE



CPU VLDT:1.4A  
CPU VDDR:1.75A  
NB VDDHTTX:0.25A  
SB VDD:0.6A  
SB PCIE VDDR:0.8A  
SB AVDD SATA:0.5A

**TOTAL:5.3A**

080902 change to TO252 package	SB700 VCore >1.17V. Data corruption may happen if less than 1.17V
--------------------------------	--

080909 add



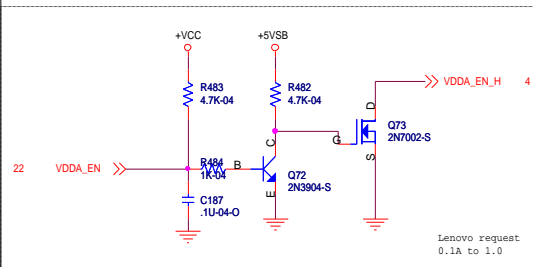


# ATHLON64 POWER GOOD & ENABLES CIRCUIT

2009 6 6 V0.1  
Del reserved  
AMD Power sequence  
function

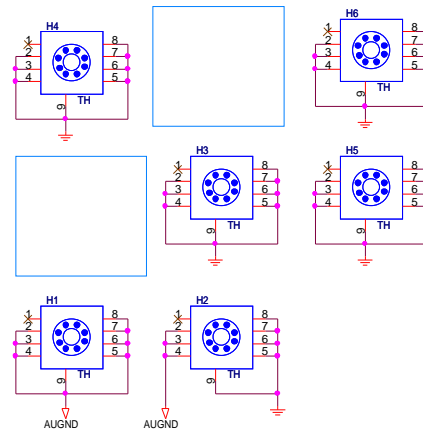
2009 6 6 V0.1  
Move D3MM\_STL\_EN Pull high +5VSB R393 to Page 28  
for Del reserved  
AMD Power sequence  
function

2009 6 6 V0.1  
Del H7,H8 for PCB SIZE change to 244\*224mm

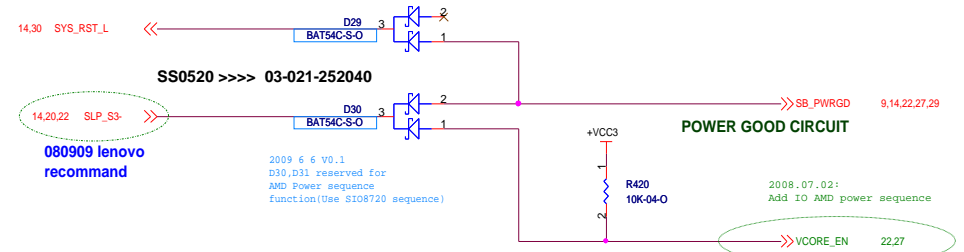


Lenovo request  
0.1A to 1.0

2009 6 6 V0.1  
Del minimum load function



# POWER GOOD & ENABLES



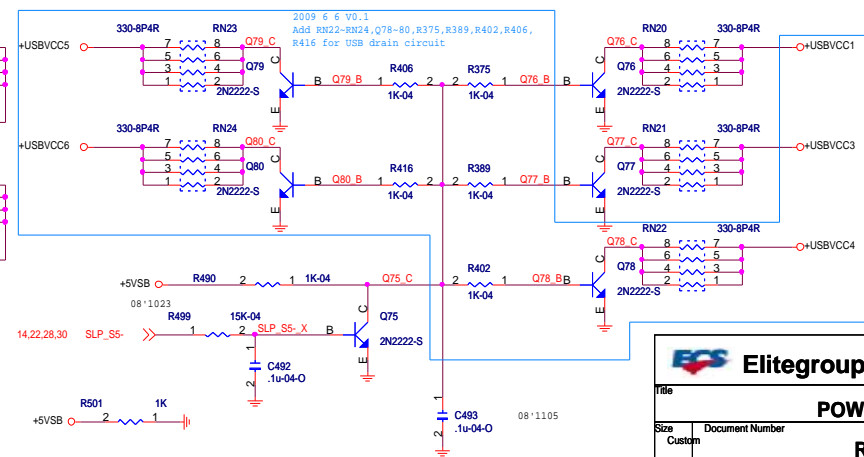
SS0520 >>>> 03-021-252040

080909 lenovo  
recommand

2009 6 6 V0.1  
D30,D31 reserved for  
AMD Power sequence  
function(Use SIO8720 sequence)

POWER GOOD CIRCUIT

2008.07.02:  
Add IO AMD power sequence



Elitegroup Computer Systems			
POWER ENABLE			
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## SB710

Name	Type	Voltage	Default	Functional Description	Function
GPIO4	I/O	3.3V	Input	Smartvolt Select 1/Serial ATA Interlock 2/GPIO 4	H_PRESENT_L
IMC_GPIO8	I/O	3.3V_S5	Input	IMC_GPIO8	F_USB1 detect
IMC_GPIO9	I/O	3.3V_S5	Input	IMC_GPIO9	F_USB2 detect
IMC_GPIO10	I/O	3.3V_S5	Input	IMC_GPIO10	F_USB3 detect
IMC_GPIO11	I/O	3.3V_S5	Input	IMC_GPIO11	LC CLR_CMOS
IMC_GPIO13	I/O	3.3V_S5	Input	Low Voltage SMBus Clock 3/IMC_GPIO13	SMCLK3
IMC_GPIO14	I/O	3.3V_S5	Input	Low Voltage SMBus Data 3/IMC_GPIO14	SMDATA3
GPIO5	I/O	3.3V	Input	SMARTVOLT2/SHUTDOWN#/GPIO5	F_AUDIO detect
GPIO9	I/O	3.3V	Input	DDC1_SCL/GPIO9	N/A
GPIO8	I/O	3.3V	Input	DDC1_SDA/GPIO8	N/A
GPIO66	I/O	3.3V_S5	Input	Low-Low Battery/GPIO 66	LPCPD_N
GPIO13	I/O	3.3V	Output	LAN DAM function	GP013
GPIO31	I/O	3.3V_S5	Input	LAN DSM function	GPI31

## ITE8720

Name	Type	Voltage	Functional Description	Function
GP14	I/O	5V	Serial VID clock/PECI request/GPIO14	COM2 detect
GP22	I/O	5V_S5	Serial flash clock/GPIO22	Power LED
GP23	I/O	5V_S5	Serial flash in data/GPIO23	SUS LED
GP30	I/O	5V	Voltage ID0/GPIO30	BEEP
GP31	I/O	5V	Voltage ID1/GPIO31	BIOS reserve
GP34	I/O	5V	Voltage ID4/GPIO34	BIOS reserve
GP35	I/O	5V	Voltage ID5/GPIO35	BIOS reserve
GP40	I/O	5V_S5	3VSB SW/GP40	Dual switch
GP33	I/O	5V	VID3/GP33	Sensor header ID1
GP47	I/O	5V	IR output/GP47	Sensor header ID2
GP50	I/O	5V	Serial flash data output/GPIO50	BIOS reserve

## For 103

X1(WIRE1)  
XTAL-JW

SPI\_ROM\_D(104)1  
SPI-ROM-D-8M

BT1(104)1  
+ KTS  
LITHIUM BATTERY  
CD2032  
BATTERY

CLR\_CMOS1(104)1  
JP-R-H

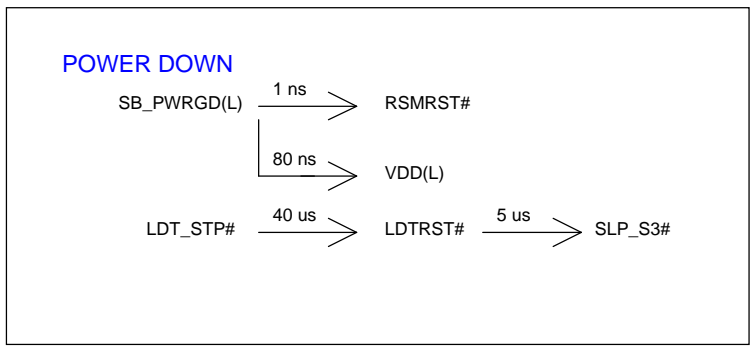
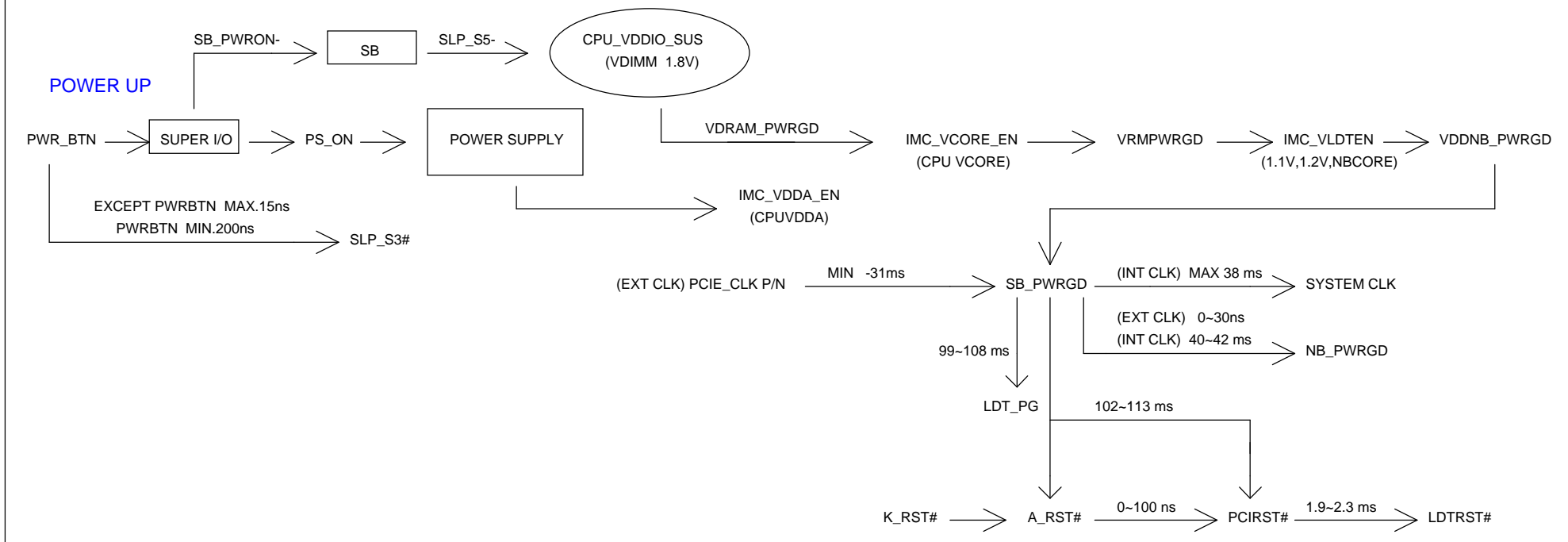
SPI\_DEBUG(104)1  
JP-R-H

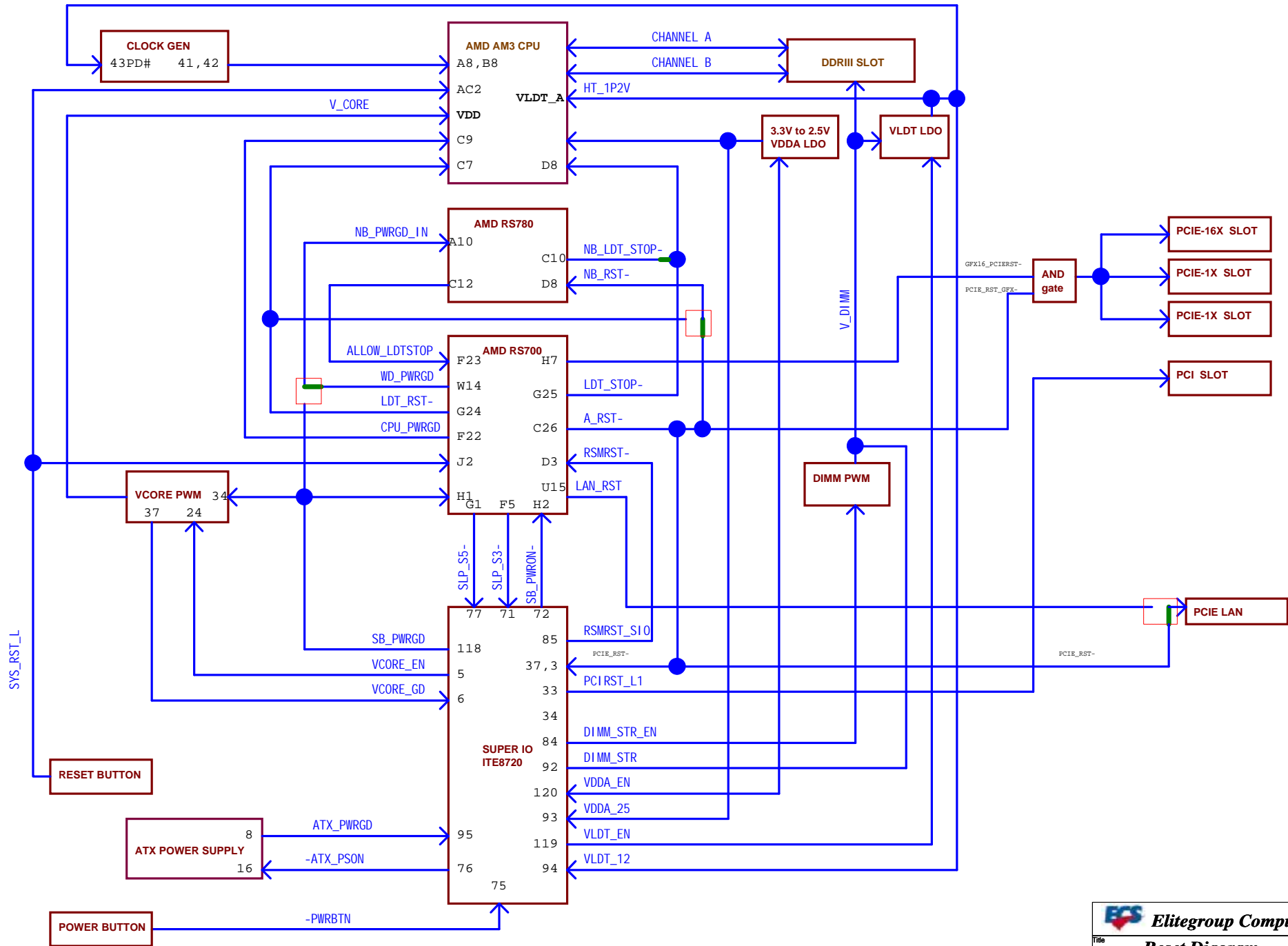
## For 104

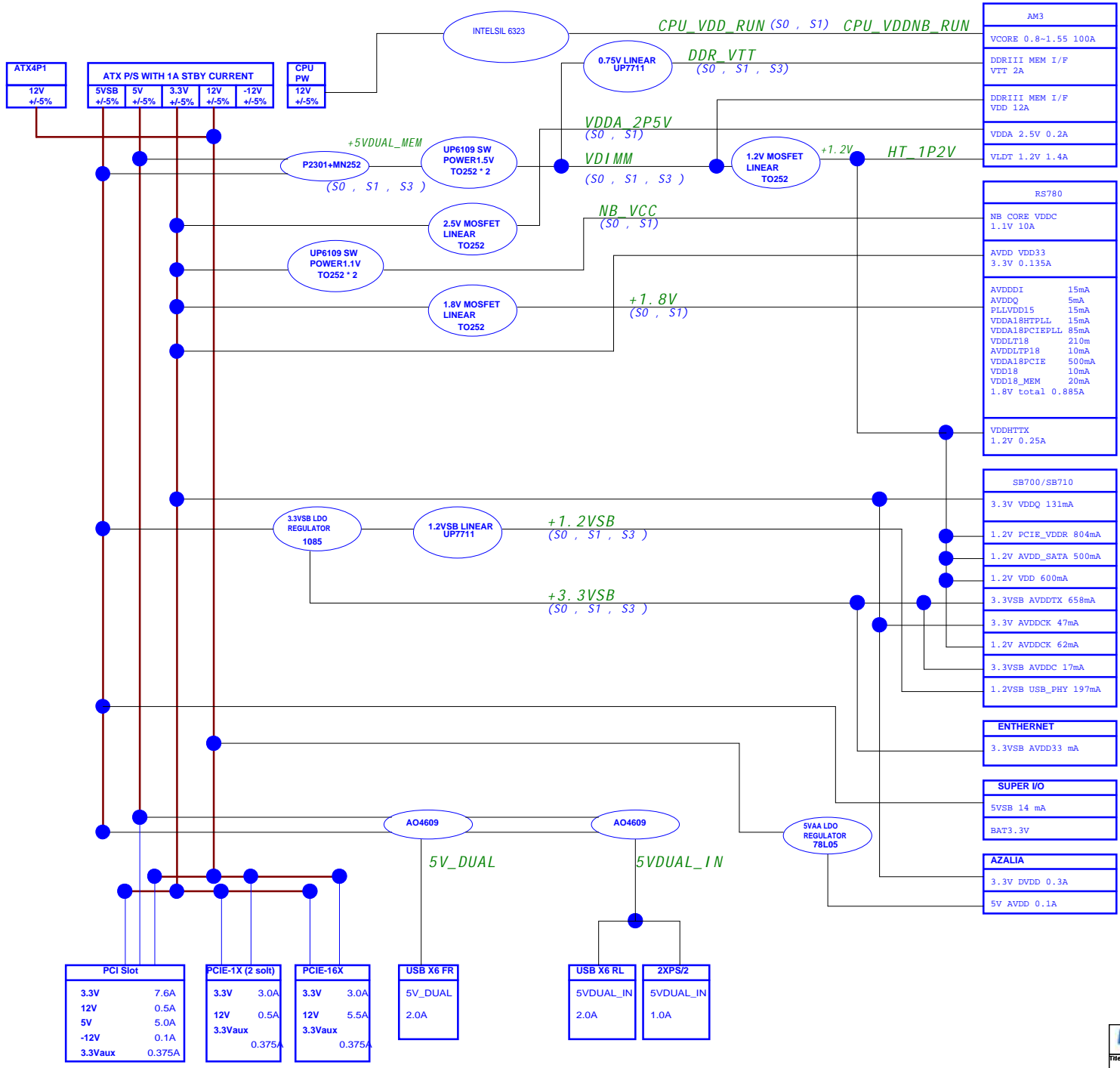
NB1(104)1  
20-120-014500  
NB\_HEATSINK\_PCCHIP

SB1(104)1  
20-120-010773  
SB\_HEATSINK\_PCCHIP

<b>ECS Elitegroup Computer Systems</b>			
Title		Attention	
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AM3	
VCORE	0.8~1.55 100A
DDRIII MEM I/F	VTT 2A
DDRIII MEM I/F	VDD 12A
VDDA	2.5V 0.2A
VLDT	1.2V 1.4A

RS780	
NB CORE VDDC	1.1V 10A
AVDD VDD33	3.3V 0.135A
AVDDDI	15mA
AVDDQ	5mA
PLLVD15	15mA
VDDA18HTPLL	15mA
VDDA18PCIEPLL	85mA
VDDLTI8	210m
AVDDLTP18	10mA
VDDA18PCIE	500mA
VDDI8	10mA
VDDI8_MEM	20mA
1.8V total	0.885A
VDDHTTX	1.2V 0.25A

SB700/SB710	
3.3V VDDQ	131mA
1.2V PCIE_VDDR	804mA
1.2V AVDD_SATA	500mA
1.2V VDD	600mA
3.3VSB AVDDTX	658mA
3.3V AVDDCK	47mA
1.2V AVDDCK	62mA
3.3VSB AVDDC	17mA
1.2VSB USB_PHY	197mA

ENTHERNET	
3.3VSB AVDD33	mA

SUPER I/O	
5VSB	14 mA
BAT3.3V	

AZALIA	
3.3V DVDD	0.3A
5V AVDD	0.1A

PCI Slot	
3.3V	7.6A
12V	0.5A
5V	5.0A
-12V	0.1A
3.3Vaux	0.375A

PCI-E 1X (2 slot)	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.375A

PCI-E 16X	
3.3V	3.0A
12V	5.5A
3.3Vaux	0.375A

USB X6 FR	
5V_DUAL	
2.0A	


USB X6 RL	
5VDUAL_IN	
2.0A	

2XPS2	
5VDUAL_IN	
1.0A	

## REVISION HISTORY:

Rev	Date	Notes
0.1	09'0606	<p><b>Change from RS780Q-LM2 V1.0 modify reserve function to meet RS780Q-LM3 V0.1 Spec.</b></p> <p><b>Page 3</b> 1.Change DIMM01,B1 net to test port for SPEC. change</p> <p><b>Page 4</b> 1.Del FB17,R282,R248,R292 for cost down 2.Del Q36,R263,R240,R269,R251,R248 for The Side Band Interface bus is not used 3.Change R264 from 300 to 1K for The Side Band Interface bus is not used 4.Del Q35,R26,R286,Q37,R266,C252,R250,R249,C260,Q33,R223,C255,R222,Q32,C254 reserved level shift function 5.C65,RN8 reserced for cost down</p> <p><b>Page 5</b> 1.C444,SC58 reserced for cost down 2.Add C507,C508 and reserved for AMD checklist 3.C456 stuff for AMD suggest</p> <p><b>Page 6</b> 1.C370,C371,C380 reserved for SI 2.C499,C500 stuff for AMD NB Schematic Checklist</p> <p><b>Page 7</b> 1.Del 2 DIMM slot for SPEC. and shift page</p> <p><b>Page 9</b> 1.Del FB15,CL15,Q12,R138,R147,R156,R155,R146,R137,R145,R169,R126,R125,R124,SFB7,R121 R118 : Change RJ3,RJ4 to R120,R142 for not Co-Lay RS740 2.Del SR1: Reserve R127,U17,SC13,SC6: Stuff R119,R466 for cost down 3.Change SC7,SC8 from 10uF to 2.2uF for AMD Schematic Review Checklist 4.Del R119,U17,C461,R127,R466,for AMD confirm NB_PWRGD_IN can cost down 5.Del PinA19-B17 Net for DVI Single-Link (RS760 only support Single-Link)</p> <p><b>Page 10</b> 1.Del RJ2,RJ7,RJ1,RJ6,SR2,SR5,R143: Add R145,R146 for not Co-Lay RS740</p> <p><b>Page 11</b> 1.Del R195,RJ9 for not Co-Lay RS740 2.Del SR12,FB22,SFB5,SR11,R159,SR19: Reserve SC31for cost down 3.Change SC29,SC32 from 22u to 10u for AMD NB Schematic Checklist</p> <p><b>Page 12</b> 1.Del RJ8: Add R195 for not co-Lay RS740 2.Del Q28,Q29,R187,R192,,R186,R191,R447-R464: Reserve C193,C186 for cost down</p> <p><b>Page 13</b> 1.Del R424,R443,R485,R506,R50,R508,R437,R509 for cost down 2.Del Net INTRUDER_L for del case open function</p> <p><b>Page 14</b> 1.Del Net SC1K3,SDATA3 The Side Band Interface bus is not used and del ohm for cost down 2.Del Net USB_P8,USB_P9,SVDUAL_IN_OC2 for del 2 USB port 3.Del Net GPIO24,GPIO25,,LPCPD_N for del TPM function 4.Del R367,R319 for not co-Lay RS740</p> <p><b>Page 15</b> 1.Del SC122,SC118,SC123,SC117 for AMD confirm can cost down for no use IDE</p> <p><b>Page 16</b> 1.Del eSATA function 2.Del Net C476,C477 for del eSATA port 3.Del R323,R327 for cost down</p> <p><b>Page 17</b> 1.Del RJ14,RJ15 for cost down</p> <p><b>Page 18</b> 1.Del Q7,R71,Q6,R70 for not co-Lay RS740 2.Del CHOCKE17,CHOCKE18,CHOCKE23,U5,SC140,SC141,U9 for DVI Single-Link (RS760 only support Single-Link) 3.Del Q2,R46,R55,Q3,R59,R47 for not co-Lay RS740</p> <p><b>Page 19</b> 1.Del R173,R172,R181,R188 for not co-Lay RS740 2.Del R205,R304: reserved EC23 for cost down</p> <p><b>Page 20</b> 1.Del F4,SD14,EC9,C75,CHOCKE5,CHOCKE6,U11,SC3: Change USB1 from 4 Port to 2 Port 2.Del U24,R336,R338,R344,R346,R350,R353,R357,R341,R487,R486,R337,R349,R352,R325,R358, BC11,EEP3,R332,C334,C329,C341,C344,C343,C348 for SPEC. del TPM function</p> <p><b>Page 21</b> 1.Change EC25 from 1000U to 220U Change EC42 from 1000U to 22U for cost down</p> <p><b>Page 22</b> 1.Del FDD for SPEC. del FDD function 2.Del R479,R510,C488,R480,Q71,Q70,R481 for del RSMRST function 3.Change R406,R444,R471 to RN13 for cost down 4.Del R423,R422,C440 monitor function 5.Del CMS-OPEN for SPE. del case open function 6.Thermal diode and SEN_HEADER PIN2 Connect to SIO PIN 87 TS_D- 7.Del ER11,ER10,C441,C442 for SPEC. only reserve VCORE</p> <p><b>Page 23</b> 1.COM1 Port change to header, COM2 Port change to connector and reserved</p> <p><b>Page 24</b> 1.Del R54(Rf),R66(Rb),R78(Rd),R87,Q10,C70,C62,C74,C80(Mb),EEP1,C7,C4(Eb) for not co-layout 88B8070 2.Del R28 for vendor confirm can cost down 3.Change C71 from 4.7u to 10u for vendor review suggest</p> <p><b>Page 25</b> 1.Change EC11,ECS from EC100U to SMD4.7U-08 of C44,C46: Change R40,R10,R19,R74 from 2.2K to 4.7K and reserved D4,R40,R10 for vendor review no use retasking 2.Del R37of not supply AC'97 function 3.Del Net SPDIF_OUT1 for SPEC. del SPDIF_OUT function 4.Del C46,C60,R101 for SPEC. del MONO OUT function</p> <p><b>Page 26</b> 1.Del R3,R2,C2,C1,R1,R6,C19,U1,R4,D3,MONO_OUT,D2,C22 for SPEC. del MONO OUT function 2.Del Q1,R114,C104,R113 of not supply AC'97 function 3.Del R13,C105,C89,R151,SPDIF_HEADER for SPEC. del SPDIF_OUT function</p> <p><b>Page 28</b> 1.Change EC50 470u to 220u for cost down</p> <p><b>Page 29</b> 1.Del RN4,R203 for not Co-Lay RS740 2.Del Q47:hange EC36 from 470U to 220U for cost down 3.Change VREF2.5V source from +3.3VSB to +VCC3 for +3.3VSB Loading</p> <p><b>Page 30</b> 1.Del PWR_FAN,R498,C217,EC39,R493,D40,R228,R243 for SPEC. del PWR_FAN function</p> <p><b>Page 31</b> 1.D29,D30 reserved for AMD Power sequence function(Use SIO8720 sequence) 2.Del R500,Q78 for del reserved minimum load function 3.Add R375, R389 for USB drain circuit 4.Del H7,H8 for PCB SIZE change to 244*224mm</p>

Rev	Date	ECN no.	Notes
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